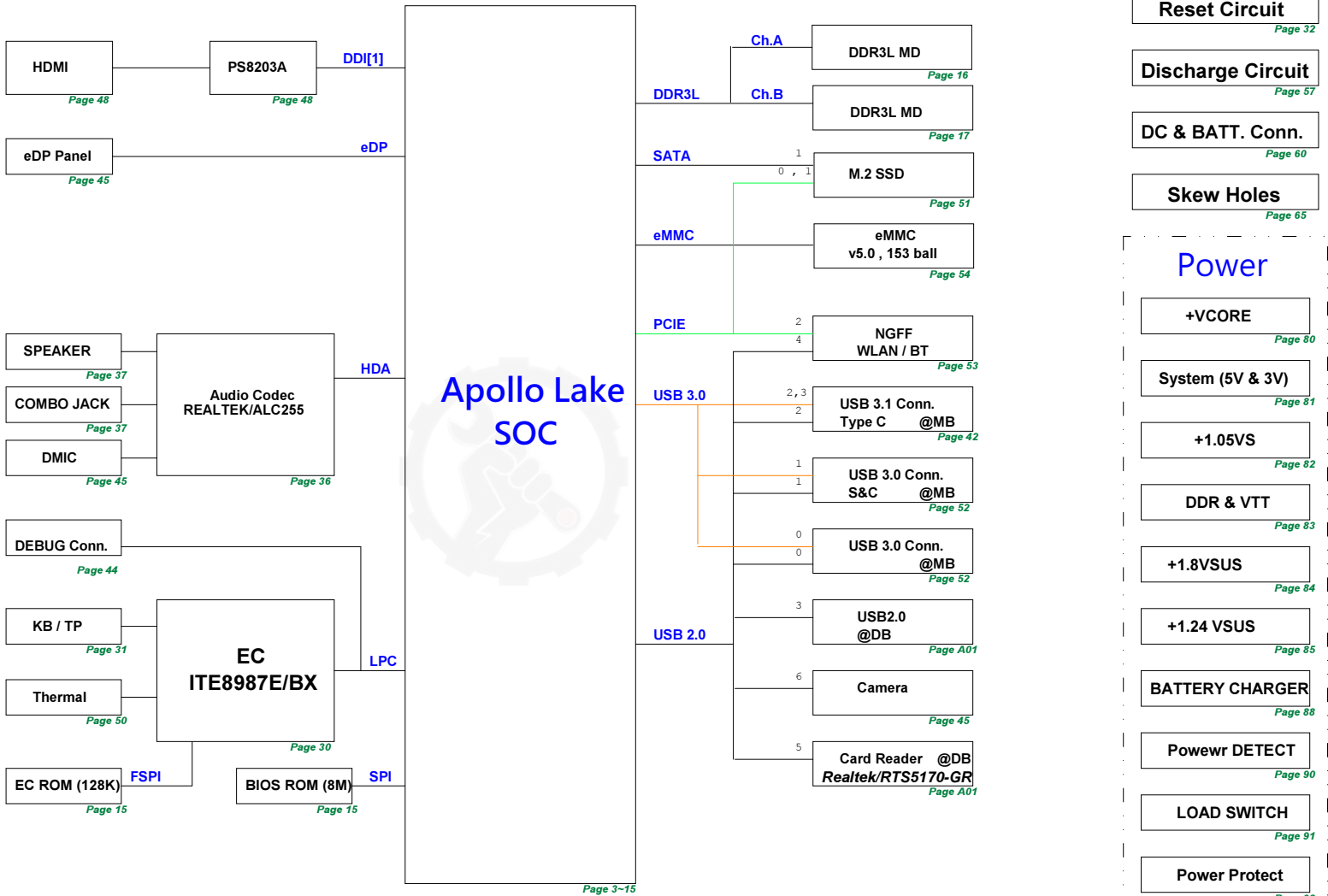


# Armani with Intel Apollo Lake Block Diagram



Page Name

01. Block Diagram
03. CPU(2)_DDR3L
04. CPU(3)_USB,PCIE,SATA,SMBus
05. CPU(4)_DDI,MIPI,EMMC,SDIO
06. CPU(5)_I2C,LPC
07. CPU(6)_RTC
08. CPU(7)_GPIO
09. CPU(8)_POWER
10. CPU(9)_GND
12. CPU(10)_LEVEL_SHIFT
13. CPU(11)_APL HW STRAPS
15. CPU(13)_SPI,SMB
16. DDR3L_MEMORY DIMM
17. DDR3L_MEMORY DIMM
18. DDR voltage
30. EC ITE8987E/BX
31. TP / Keyboard
32. RST_Reset Circuit
36. Audio Codec
37. Speaker
41. USB 3.1 Type-C
44. BUG_Debug
45. eDP_output
48. HDMI
50. THERMAL
51. M.2 SSD
52. USB3.0_Charge IC
53. NGFF_WLAN/BT
55. PCIe re-Driver
57. Discharge
60. DC-IN/ Batt connector
62. TPM_NPT65x
65. ME_CONN,Skew Hole
66. IO Board CONN
69. Finger printer
80. POWER_VCORE
81. POWER_SYSTEM
82. POWER_1.05VS
83. POWER_DDR & VTT
84. POWER_1.8VSUS
85. POWER_1.24VSUS
88. POWER_CHARGER
90. POWER_DETECT
91. POWER_LOAD SWITCH
92. POWER_PROTECT
93. POWER_SIGNAL
94. POWER_FLOWCHART
97. POWER_TREE
98. POWER_HISTORY
99. POWER_SEQUENCE
A01. IO Board , CR , USB2 , LED

**<Variant Name>**

# PEGATRON

**Title :**\*\*\*\*\*

**PEGATRON PROPRIETARY AND CONFIDENTIAL**

**BG1-HW3**

**Engineer:**

## Raly Hsieh

Size

Project Name
--------------

me **AS3EA**

Rev 2.0

2.0

Monday, March 27, 2017

2

100

Date:

$$\frac{2}{2}$$

Sheet

1

of

A

B

C

D

A

B

C

D

---

5

---

4

---

3

$$\frac{2}{2}$$

1

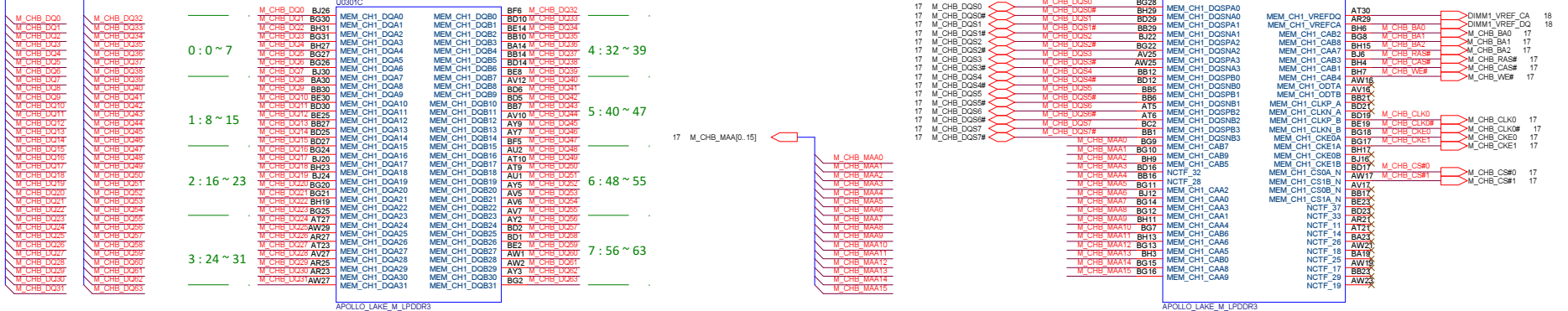
A

B

C

D

## 6 M CHA DQ[0..63]



<Variant Name>

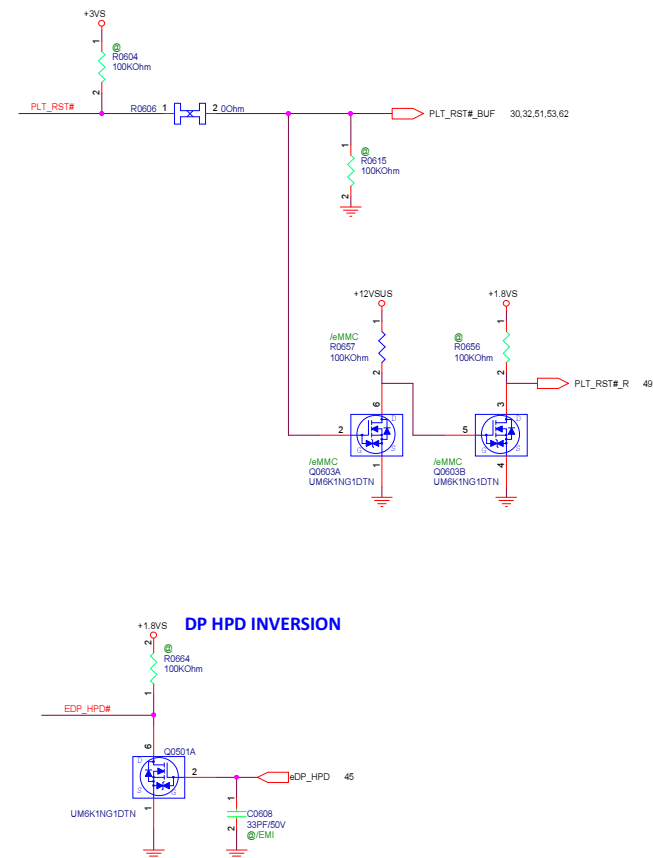
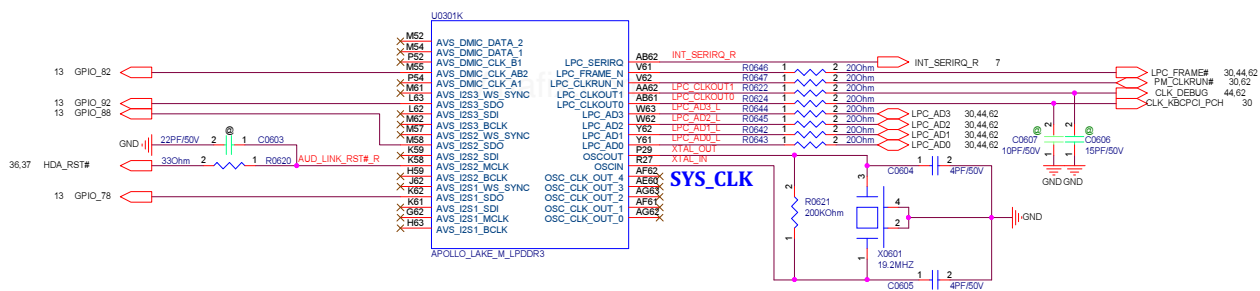
PEGATRON Title : CPU\_LPDDR3

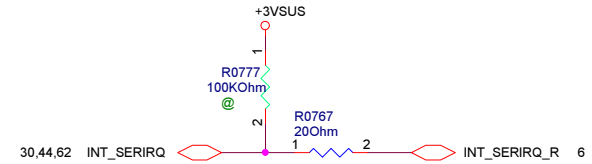
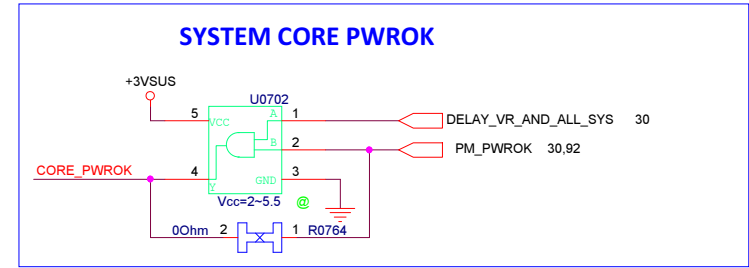
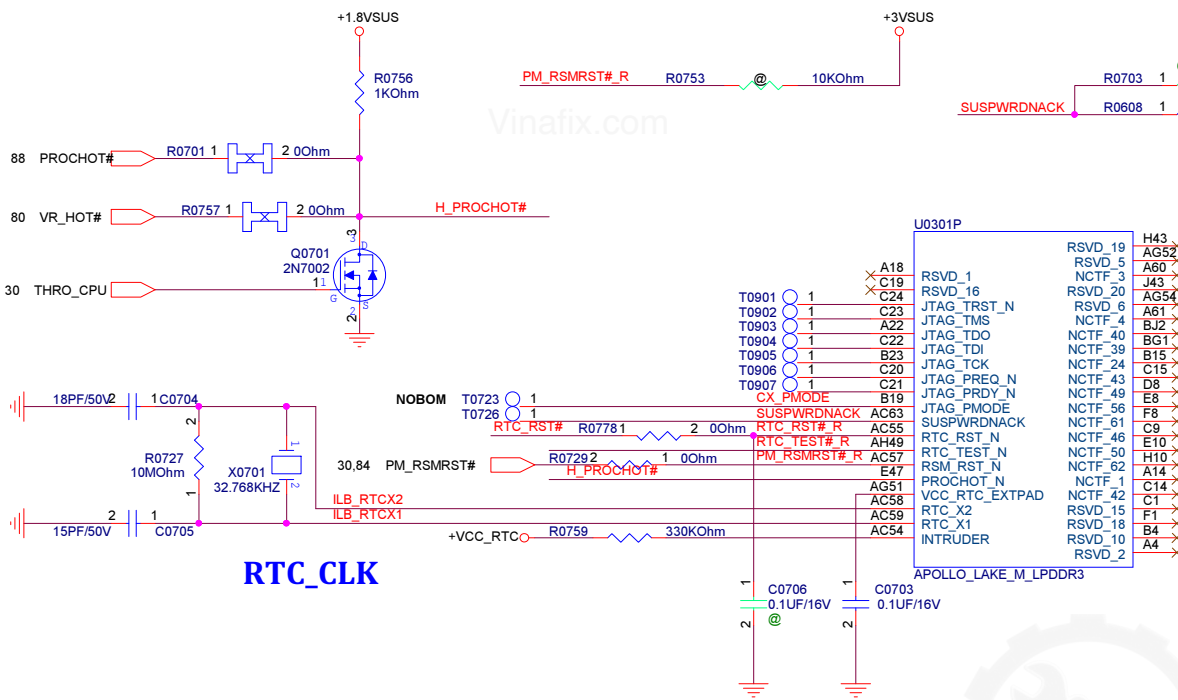
**Engineer:** Raly Hsieh

Size	Project Name
C	AS3EA
Date: Monday, March 27, 2017	Sheet 2 of 100



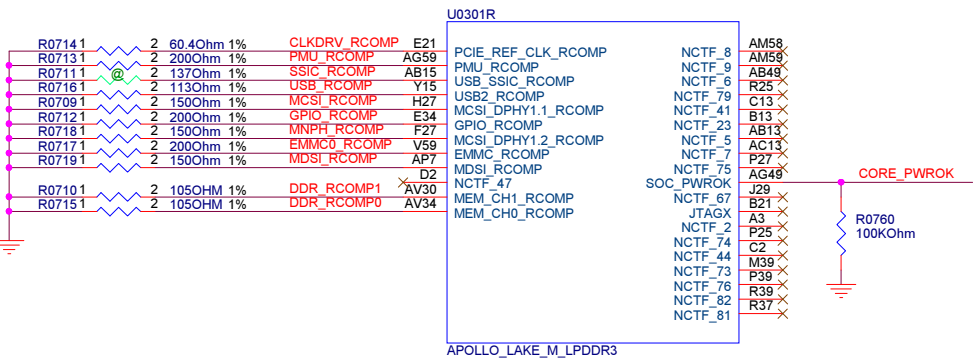
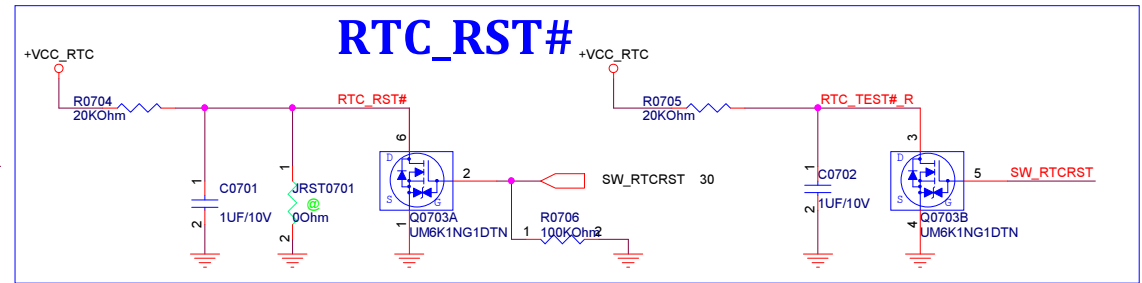






RTC\_CLK

RTC\_RST#



<Variant Name>

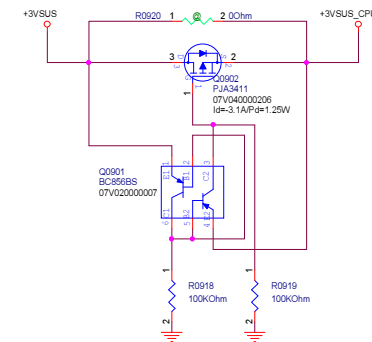
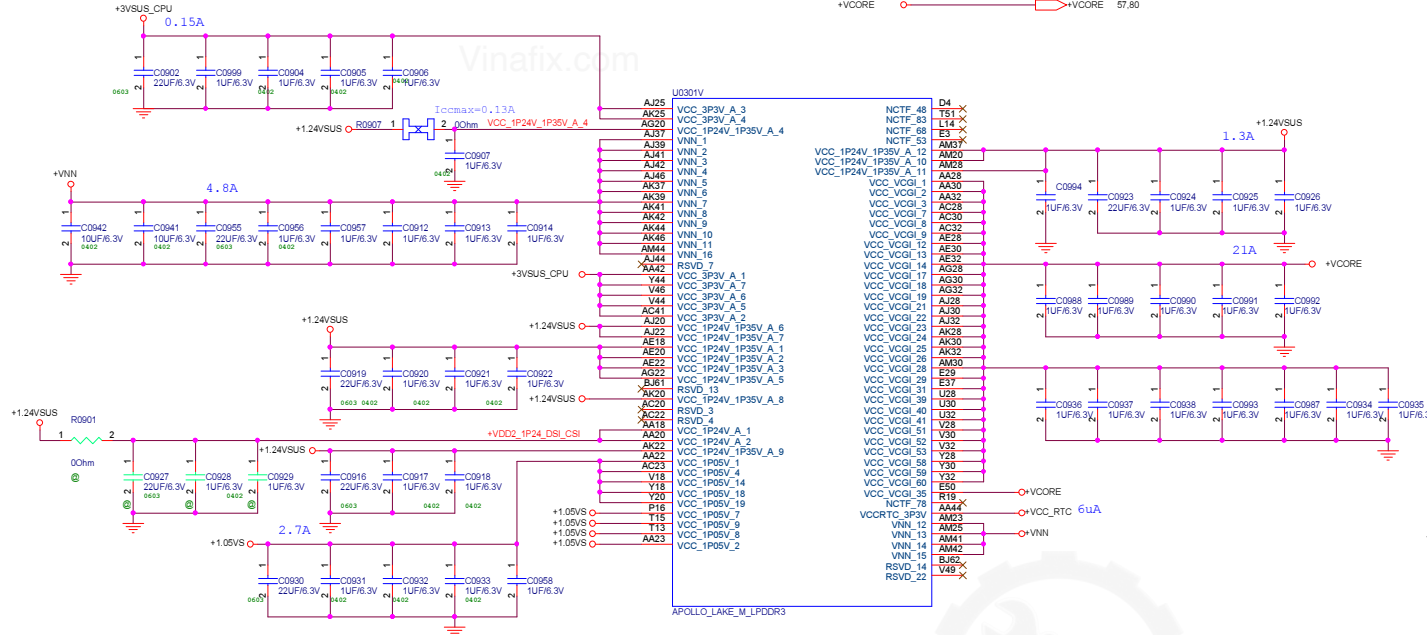
<b>PEGATRON</b>		<b>Title : RTC</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1-HW3		Engineer: Raly Hsieh	
Size	Project Name	Rev	
B	AS3EA	2.0	
Date: Monday, March 27, 2017		Sheet	7 of 100



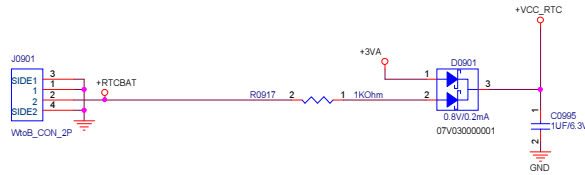
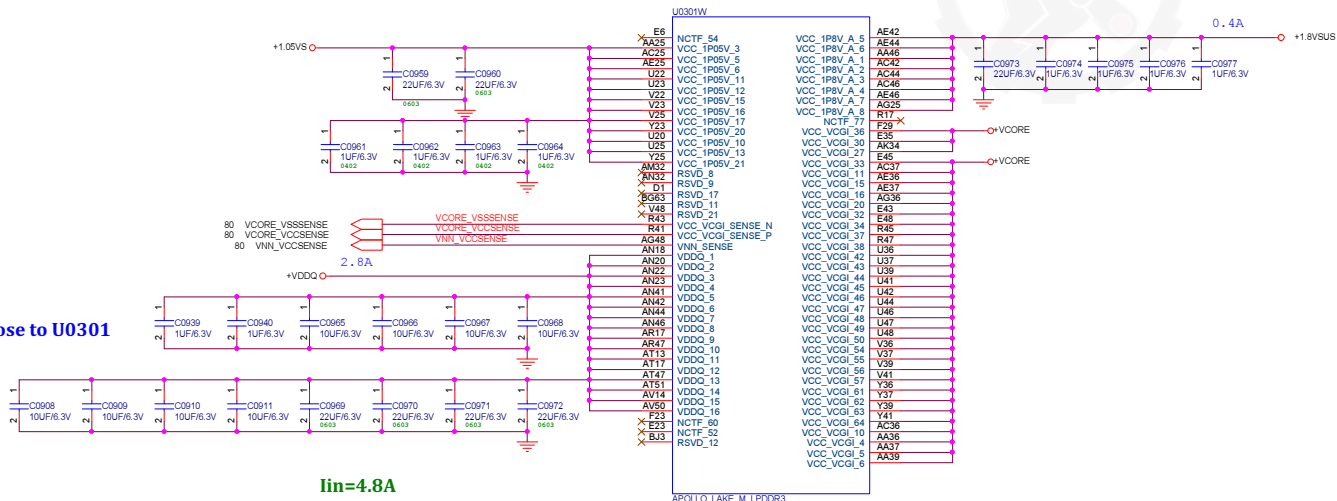


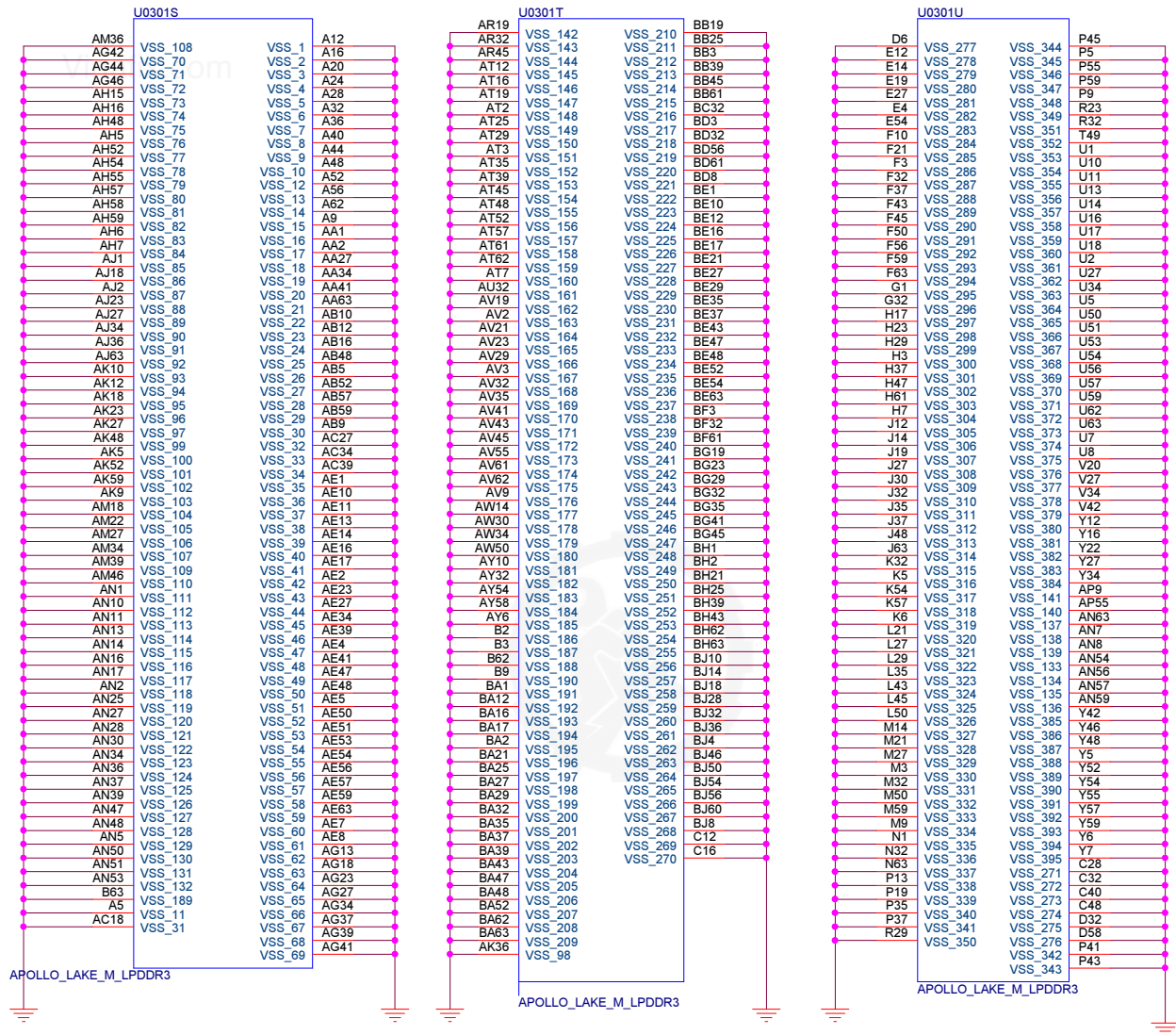
+1.05VS  
 +VNN  
 +1.8VSUS  
 +1.24VSUS  
 +3VA  
 +3VSUS  
 +VCC\_RTC  
 +VCCORE

4.57,82  
 57.80  
 4.5,6,7 & 12,13,15,44,57,84  
 57.85  
 30,31,36,53,60,65,81,88,93  
 4.67,12,15,30,31,45,53,57,62,80,81,84,85,92  
 7.36,60  
 57.80



Close to U0301





<Variant Name>

<b>PEGATRON</b>		Title : <b>CPU_GND</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1-HW3		Engineer: <b>Raly Hsieh</b>	
Size	Project Name		Rev
<b>B</b>	<b>AS3EA</b>		<b>2.0</b>
Date: <b>Monday, March 27, 2017</b>		Sheet	10 of 100

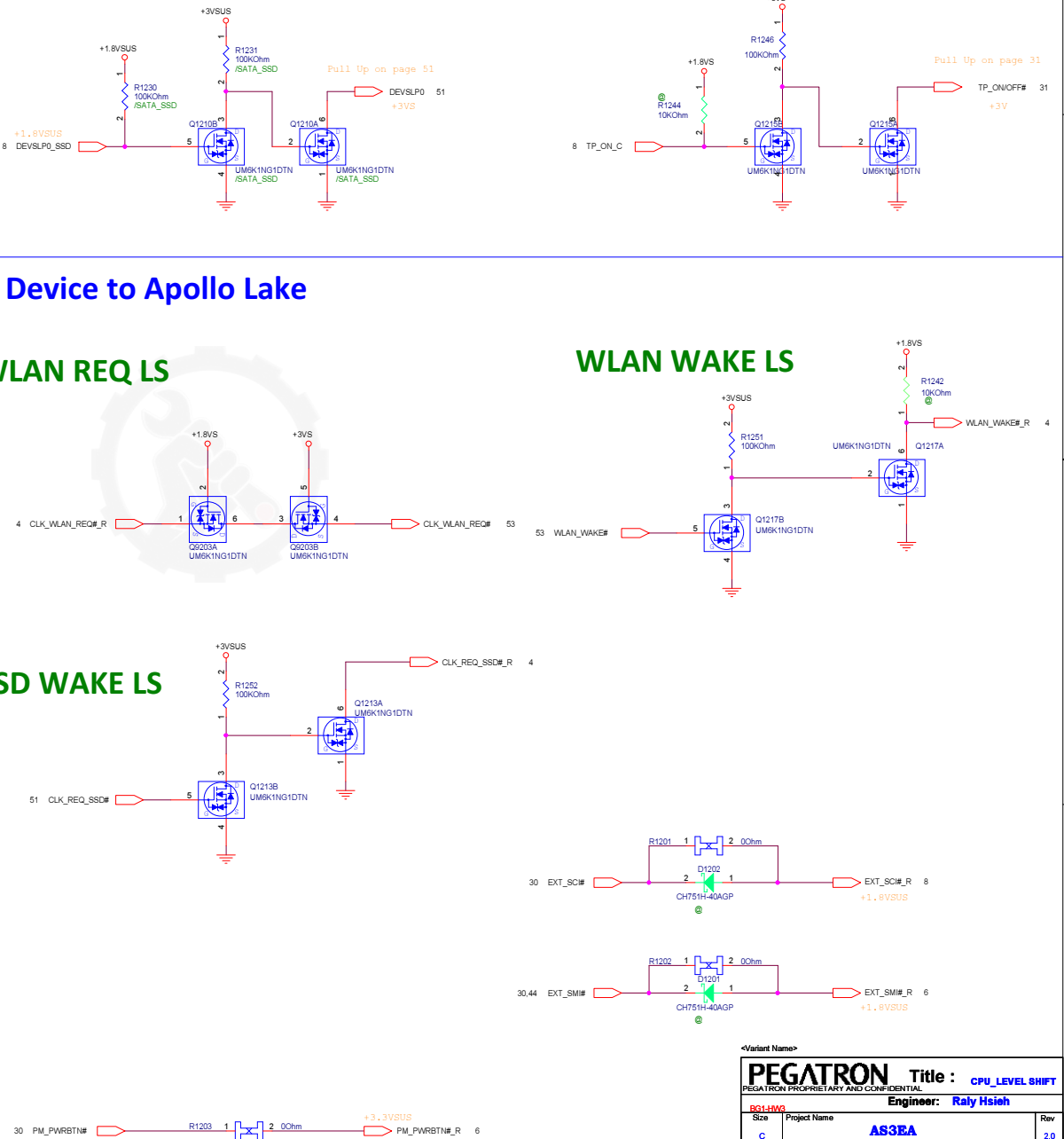
Vinafix.com



<Variant Name>			
<b>PEGATRON</b>		<b>Title :</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		<b>Engineer:</b>	
Size C	Project Name AS3EA	Rev 2.0	
Date: Monday, March 27, 2017		Sheet	11 of 100

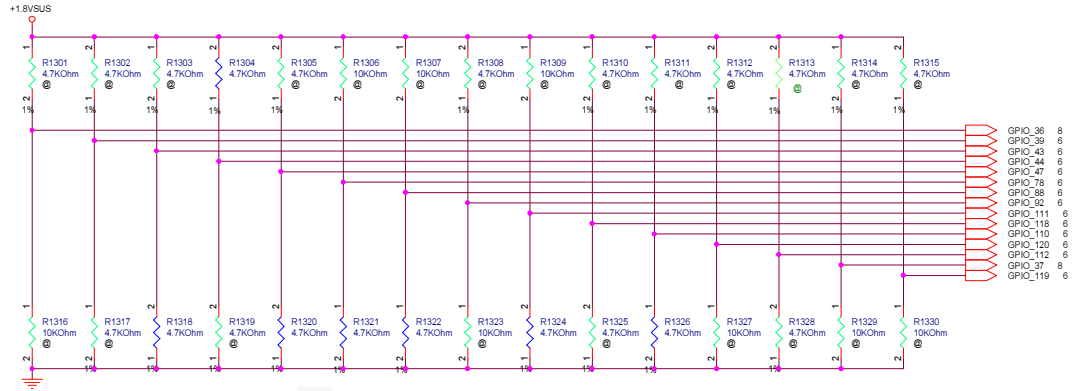
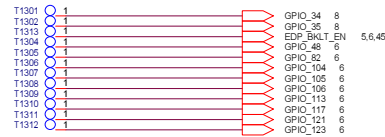
+3V	○	→	+3V	31,44,45,57,91
+3VS	○	→	+3VS	6,30,31,32,36,37,41,45,48,49,50,51,53,57,62,66,91,92
+3VSWLAN	○	→	+3VSWLAN	53
+3VSUS	○	→	+3VSUS	4,6,7,9,15,30,31,45,53,57,62,80,81,84,85,92
+5V	○	→	+5V	31,36,48,57,69,91
+12VSUS	○	→	+12VSUS	6,81,91

## SSD WAKE LS



GPIO #	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_34	RSVD	20K PD	Ensure that this strap is always pulled low for normal platform operation.
GPIO_35	RSVD	20K PD	Ensure that this strap is always pulled low for normal platform operation.
GPIO_36	RSVD	20K PD	Ensure that this strap is always pulled low for normal platform operation.
GPIO_39	Enable CSE ROM Bypass	20K PD	1 = enable bypass 0 = disable bypass (default) <b>Note:</b> 1. SoC supports TXE3.0 (this is also called CSE) 2. This strap tells CSE (TXE3.0) to bypass Read-Only Memory (ROM) that it has on SoC. If an issue occurs with the boot up code of CSE (TXE3.0) before the first patch point this strap enabled the platform tell CSE (TXE3.0) to bypass the ROM causing the issue and go to the patch space instead.
GPIO_40	RTC Clock Timer Bypass	20K PD	1 =enable bypass 0 =disable bypass (default) <b>Note:</b> This strap shall only be used when an external oscillator is used to supply a 32.768kHz clock to RTC_X1.
GPIO_43	RSVD	20K PU	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_44	Allow SPI as a boot source	20K PU	1=enable (default) 0=disable
GPIO_47	Force DNX FW Load	20K PD	1 = Force 0 = Do not force (default) <b>Notes:</b> 1. DnX: Download and Execute. 2. This strap is a recovery strap for corrupted FW image. This strap will force CSE (TXE3.0) to execute a "Download and Execute" (DnX) flow, where it would fetch firmware from a USB stick and re-flash a eMMC device. CSE (TXE3.0) can do it for BIOS part of FW, but if CSE FW itself is corrupted we need this strap.
GPIO_48	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_78	SMBus 1.8V/3.3V mode select	20K PU	1=buffers set to 1.8V mode (default) 0=buffers set to 3.3V mode
GPIO_82	RSVD	20K PD	Ensure that this strap is always pulled low for normal platform operation.

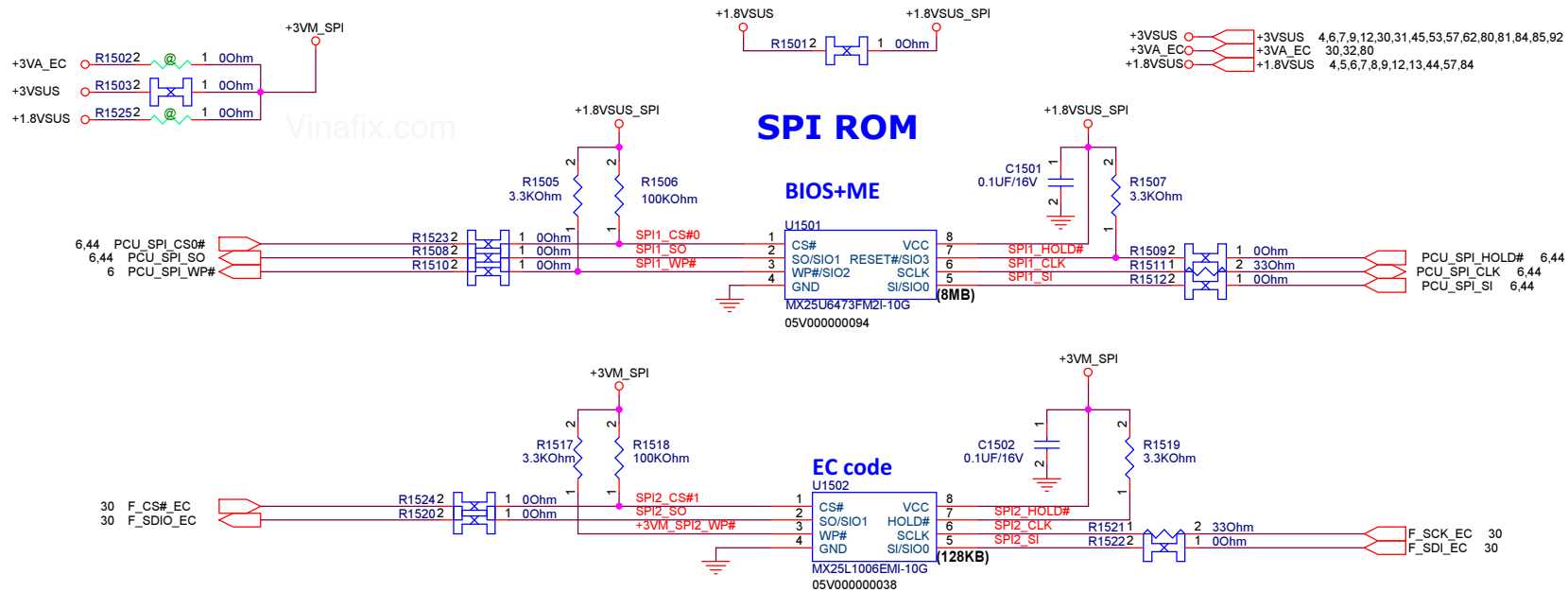
GPIO #	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_88	PMU (Power Management Unit) 1.8V/3.3V mode select	20K PU	1=buffers set to 1.8V mode (default) 0=buffers set to 3.3V mode
GPIO_92	SMBus No Re-Boot	20K PD	1 = Enable 0 = Disable (default) <b>Note:</b> Platforms should strap this LOW. Functionality is handled by the PMC.
GPIO_104	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_105	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_106	RSVD	20K PU	Ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation.
GPIO_110	LPC 1.8V/3.3V mode select	20K PU	1=buffers set to 1.8V mode (default) 0=buffers set to 3.3V mode
GPIO_111	RSVD	20K PU	<ul style="list-style-type: none"><li>Pull LOW when RSM_RST_N de-asserts to map these regions to the boot SPI</li><li>Pull HIGH when RSM_RST_N de-asserts to leave these regions unmapped by the System Agent</li></ul> <b>Note:</b> Pull LOW for designs that boot from SPI and HIGH otherwise
GPIO_112	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_113	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_117	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_118	Flash Descriptor Override	20K PD	0 = No Override (Normal Operation) 1 = Override <b>Note:</b> This strap enables the platform to override security features in the SPI.
GPIO_120	Top swap override	20K PD	1 = Enable 0 = Disable (default) <b>Note:</b> Within the SPI ROM there may be different locations where the boot code is stored. This strap enables platform to change where the core will look for BIOS code for a SPI boot only.
GPIO_121	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_123	RSVD	20K PU	Ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation.



Vinafix.com

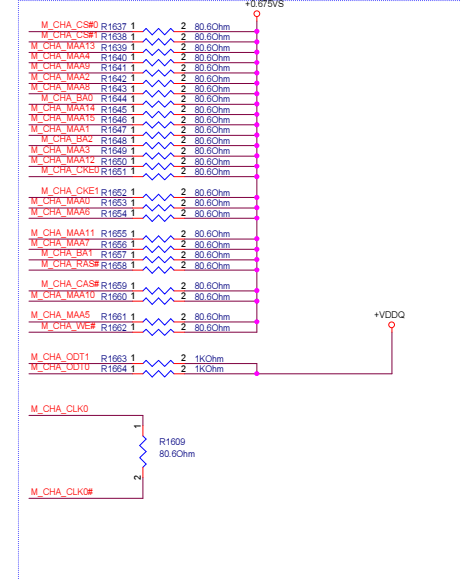
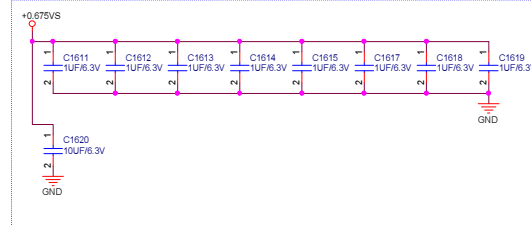
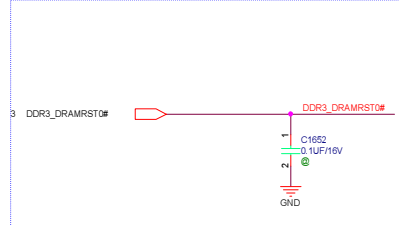
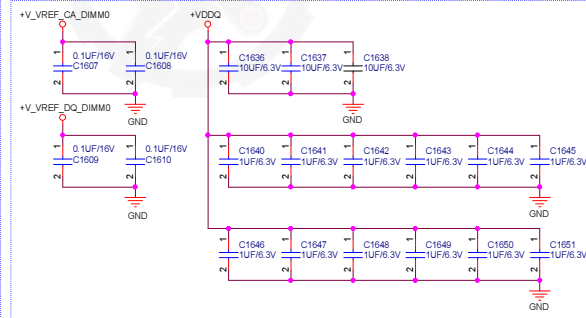
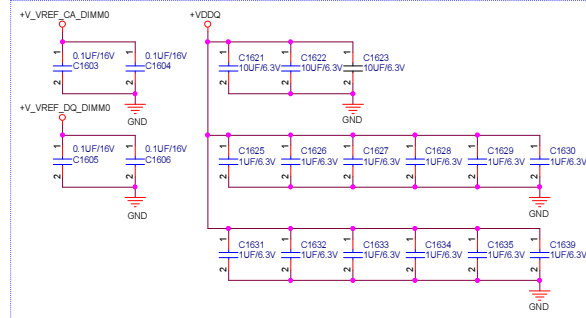
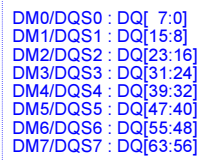
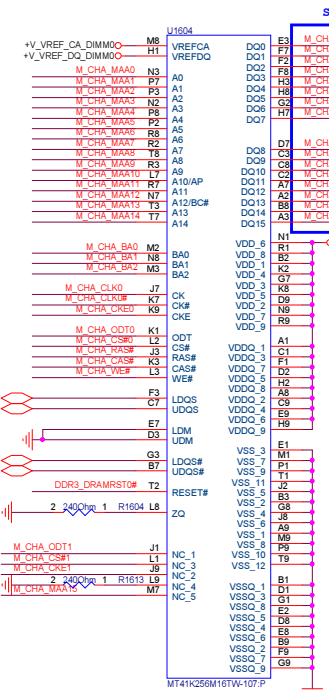
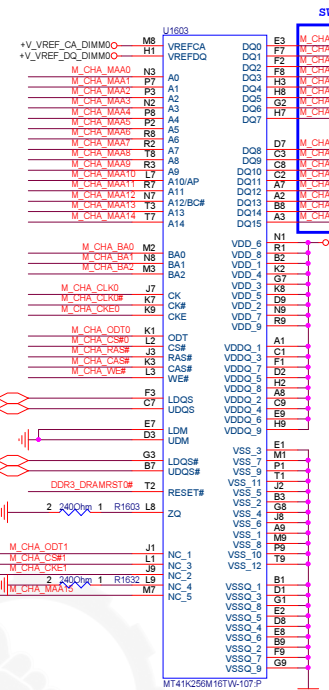
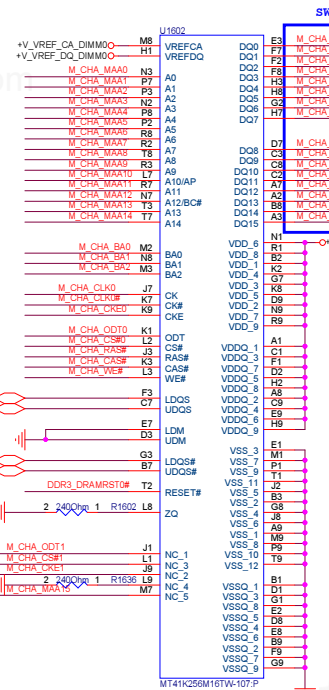
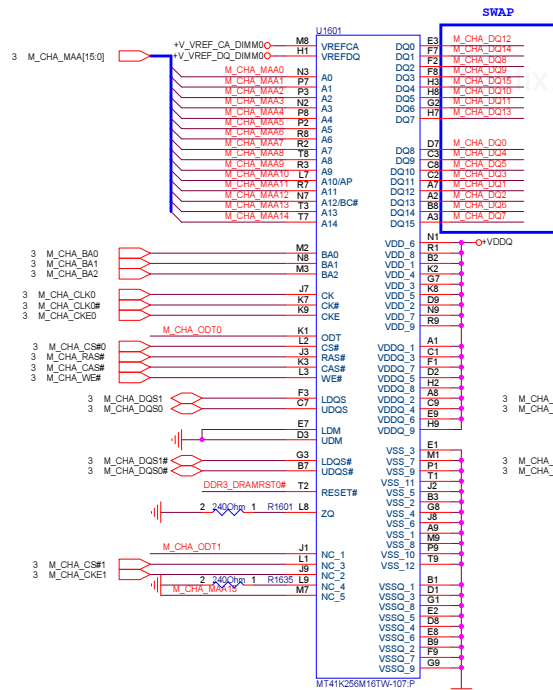


<Variant Name>			
<b>PEGATRON</b>		<b>Title :</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		<b>Engineer:</b>	
Size C	Project Name AS3EA	Rev 2.0	
Date: Monday, March 27, 2017		Sheet	14 of 100



<Variant Name>

<b>PEGATRON</b>		Title : CPU(10)_SPI	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1-HW3		Engineer: Raly Hsieh	
Size	Project Name		Rev
B	AS3EA		2.0
Date:	Monday, March 27, 2017	Sheet	15 of 100












PEGATRON PROPRIETARY AND CONFIDENTIAL **DDR3L SO-DIMM (2**  
**Engineer: Raly Hsieh**

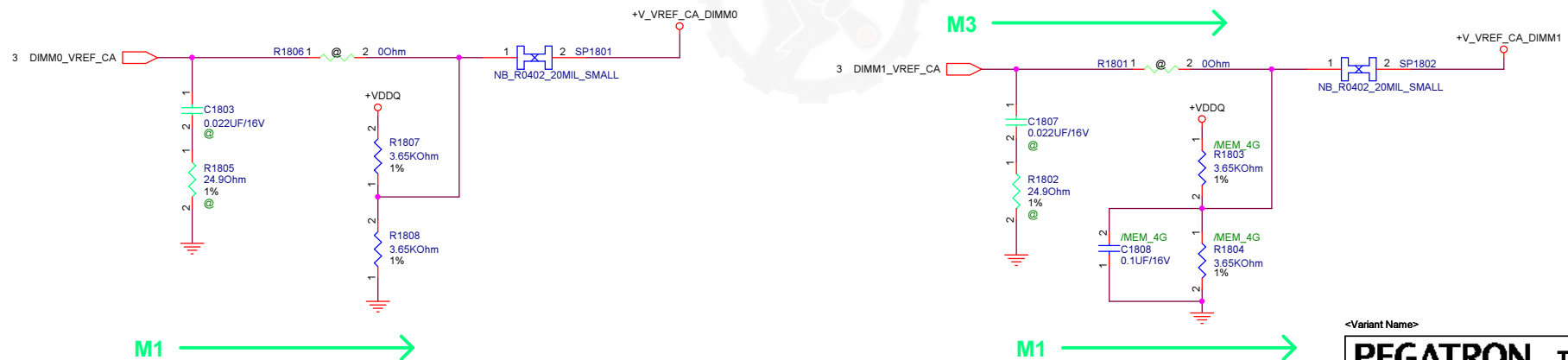
BG1-HW3		Engineer: <b>Rafiq Hsien</b>
Size	Design Name	

Size	Project Name
	<b>AS3FA</b>

C	ASSEA	
Date:	Monday, March 27, 2017	Sheet 17 of

Date:	Monday, March 27, 2017	Street:	17	City:	
1					

+V_VREF_DQ_DIMM0		+V_VREF_DQ_DIMM0	16
+V_VREF_CA_DIMM0		+V_VREF_CA_DIMM0	16
+V_VREF_CA_DIMM1		+V_VREF_CA_DIMM1	17
+V_VREF_DQ_DIMM1		+V_VREF_DQ_DIMM1	17
+VDDQ		+VDDQ	9,16,17,57,83



<b>PEGATRON</b>		<b>Title :</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL		<u>LPDDR3(3) CA/DQ Voltage</u>	
<b>BGI-HW3</b>		<b>Engineer: Raly Hsieh</b>	
<b>Size</b>	<b>Project Name</b>	<b>Rev</b>	
<b>Custom</b>	<b>AS3EA</b>	<b>2.0</b>	
<b>Date: Monday, March 27, 2017</b>		<b>Sheet</b>	<b>18 of 100</b>

Vinafix.com



<Variant Name>			
<b>PEGATRON</b>		<b>Title :</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		<b>Engineer:</b>	
Size C	Project Name AS3EA	Rev 2.0	
Date: Monday, March 27, 2017		Sheet	19 of 100

Vinafix.com



<Variant Name>			
<b>PEGATRON</b>		<b>Title :</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		<b>Engineer:</b>	
Size C	Project Name AS3EA	Rev 2.0	
Date: Monday, March 27, 2017		Sheet	20 of 100

Vinafix.com



<Variant Name>			
<b>PEGATRON</b>		<b>Title :</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		<b>Engineer:</b>	
Size C	Project Name AS3EA	Rev 2.0	
Date: Monday, March 27, 2017		Sheet	21 of 100

Vinafix.com



<Variant Name>			
<b>PEGATRON</b>		<b>Title :</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		<b>Engineer:</b>	
Size C	Project Name AS3EA	Rev 2.0	
Date: Monday, March 27, 2017		Sheet	22 of 100

Vinafix.com



<Variant Name>			
<b>PEGATRON</b>		<b>Title :</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		<b>Engineer:</b>	
Size C	Project Name AS3EA	Rev 2.0	
Date: Monday, March 27, 2017		Sheet	23 of 100

Vinafix.com



<Variant Name>			
<b>PEGATRON</b>		<b>Title :</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		<b>Engineer:</b>	
Size C	Project Name AS3EA	Rev 2.0	
Date: Monday, March 27, 2017		Sheet 24 of 100	



Vinafix.com



<Variant Name>			
<b>PEGATRON</b>		<b>Title :</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		<b>Engineer:</b>	
Size C	Project Name AS3EA	Rev 2.0	
Date: Monday, March 27, 2017		Sheet 25 of 100	

Vinafix.com



<Variant Name>			
<b>PEGATRON</b>		<b>Title :</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		<b>Engineer:</b>	
Size C	Project Name AS3EA	Rev 2.0	
Date: Monday, March 27, 2017		Sheet	26 of 100

Vinafix.com



<Variant Name>			
<b>PEGATRON</b>		<b>Title :</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		<b>Engineer:</b>	
Size C	Project Name AS3EA	Rev 2.0	
Date: Monday, March 27, 2017		Sheet	27 of 100

PCH SMBus

Vinafix.com



<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : SMBus

Engineer: Raly Hsieh

Size

Project Name

Rev

BG1-HW3

AS3EA

2.0

Date: Monday, March 27, 2017

Sheet 28 of 100

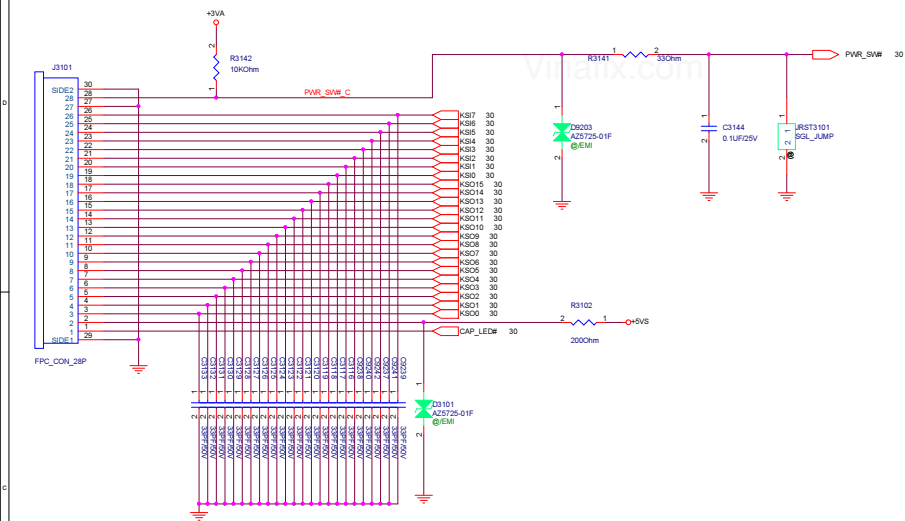
Vinafix.com



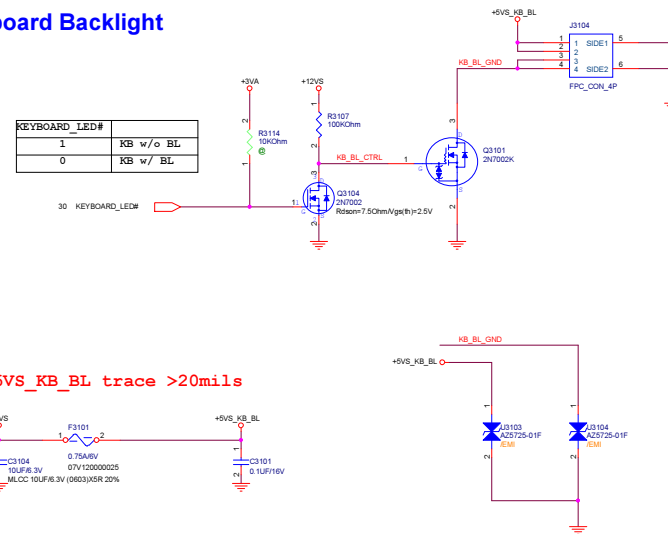
<Variant Name>			
<b>PEGATRON</b>		<b>Title :</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		<b>Engineer:</b>	
Size C	Project Name AS3EA	Rev 2.0	
Date: Monday, March 27, 2017		Sheet 29 of 100	



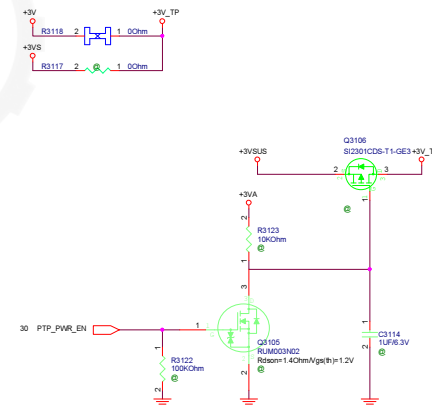
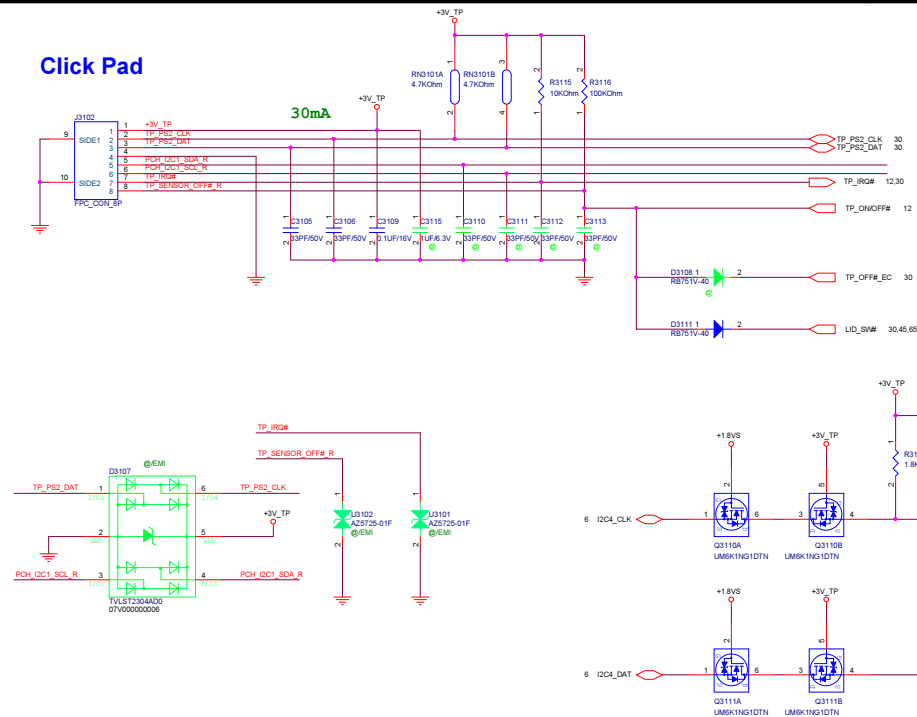
**31 KB\_TP**

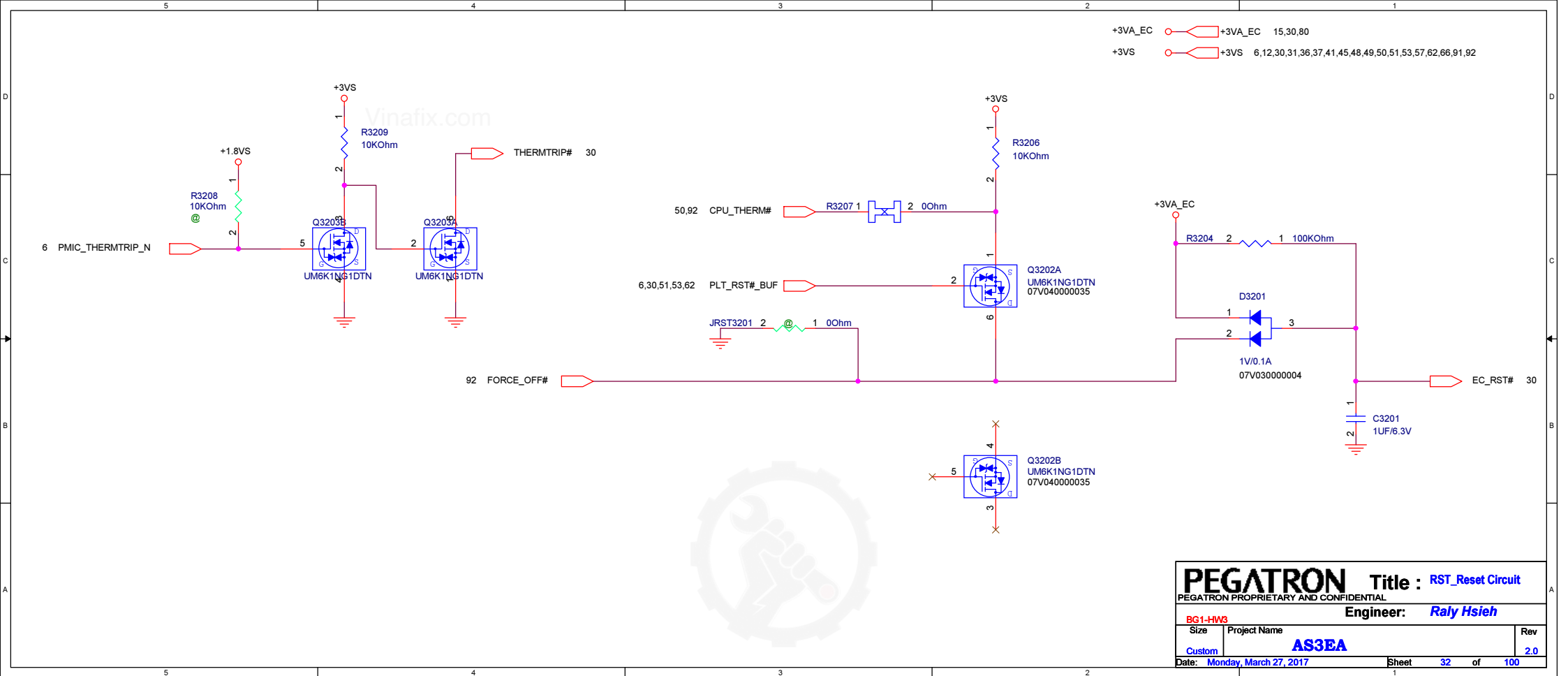


## Keyboard Backlight



### Click Pad







Vinafix.com



<Variant Name>

<b>PEGATRON</b>		Title : <b>Realtek RTL8111G</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL		<b>Raly Hsieh</b>	
BGH/HWS		Engineer:	
Size Custom	Project Name <b>AS3EA</b>	Rev 33	Rev 100
Date: <b>Monday, March 27, 2017</b>		Sheet 1 of 1	

Vinafix.com

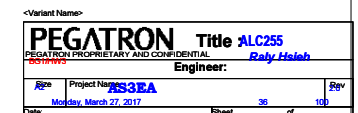


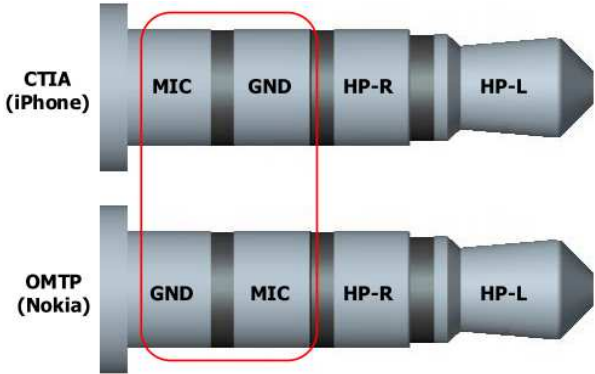
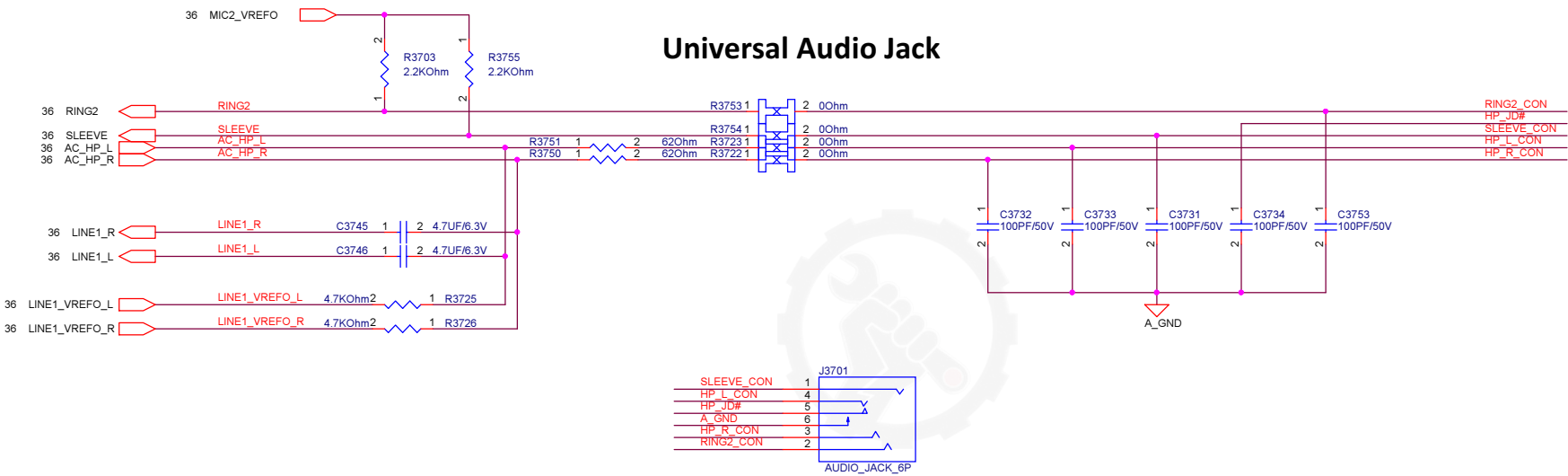
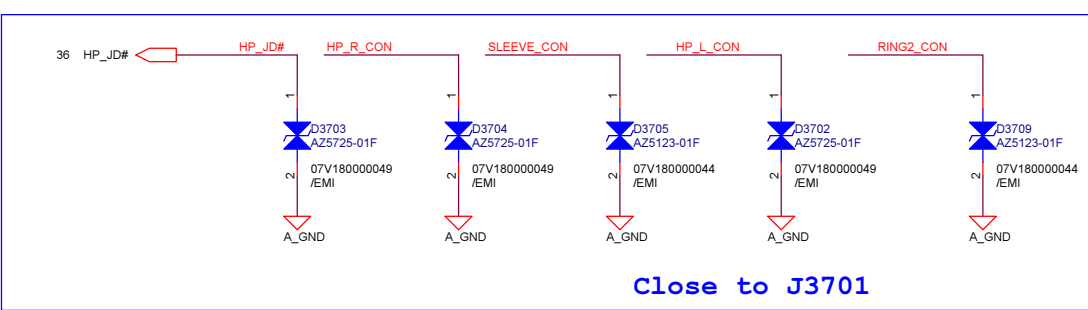
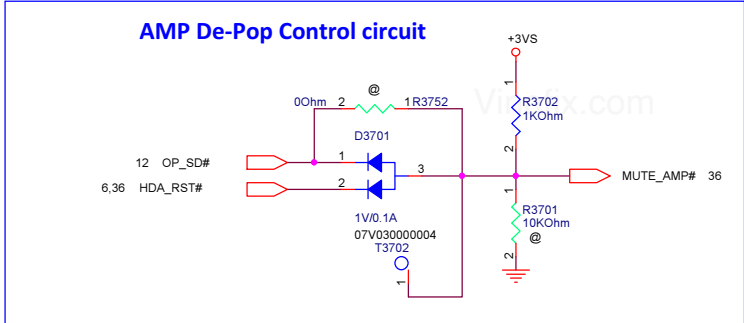
<b>PEGATRON</b>		<b>Title : RJ45</b>	
BG1/HW3		Engineer: <i>Raly Hsieh</i>	
Size Custom	Project Name <b>AS3EA</b>		Rev 2.0
Date: <i>Monday, March 27, 2017</i>		Sheet	34 of 100

Vinafix.com



<Variant Name>			
<b>PEGATRON</b>		<b>Title :</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		<b>Engineer:</b>	
Size C	Project Name AS3EA	Rev 2.0	
Date: Monday, March 27, 2017		Sheet	35 of 100





Vinafix.com



<Variant Name>			
<b>PEGATRON</b>		<b>Title :</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		<b>Engineer:</b>	
Size C	Project Name AS3EA	Rev 2.0	
Date: Monday, March 27, 2017		Sheet 38 of 100	

Vinafix.com



<Variant Name>			
<b>PEGATRON</b>		<b>Title :</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		<b>Engineer:</b>	
Size C	Project Name AS3EA	Rev 2.0	
Date: Monday, March 27, 2017		Sheet	39 of 100

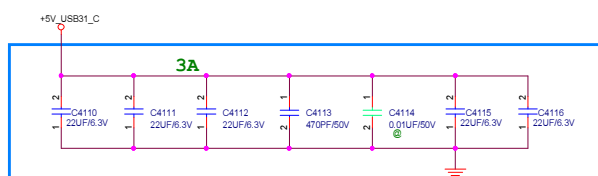
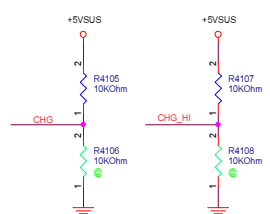
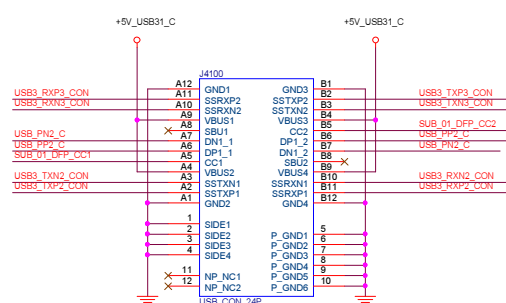
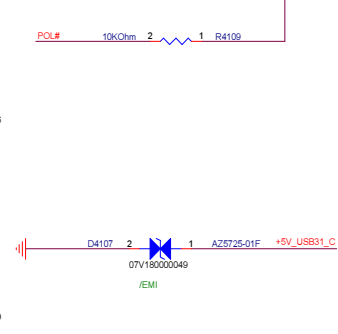
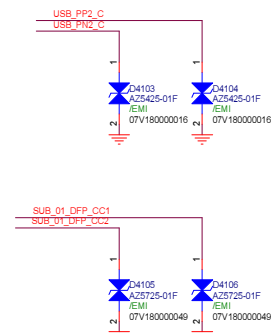
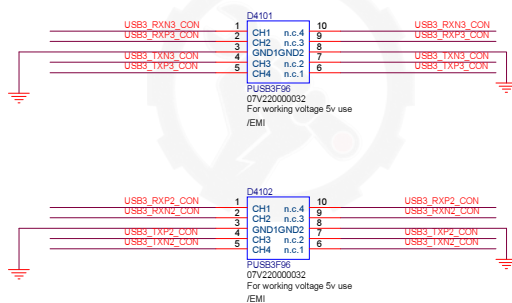
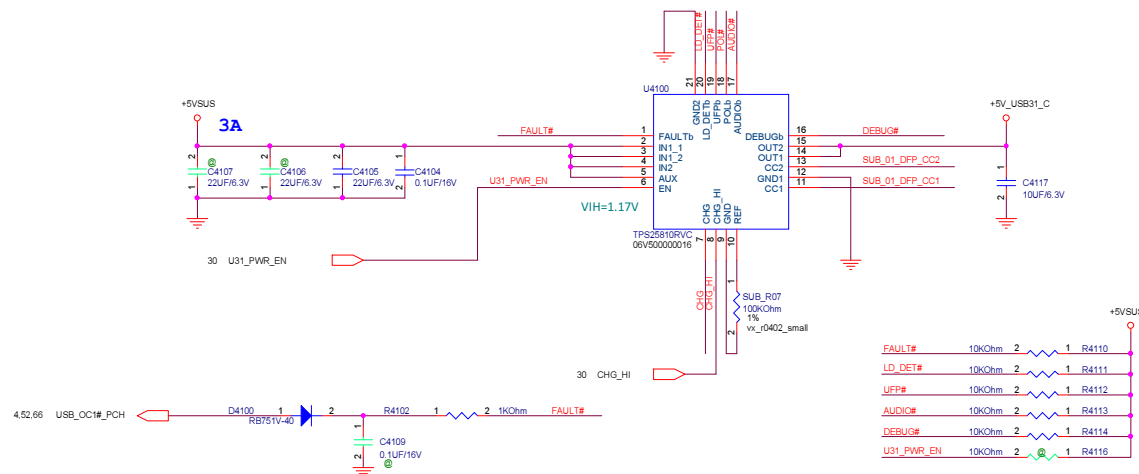
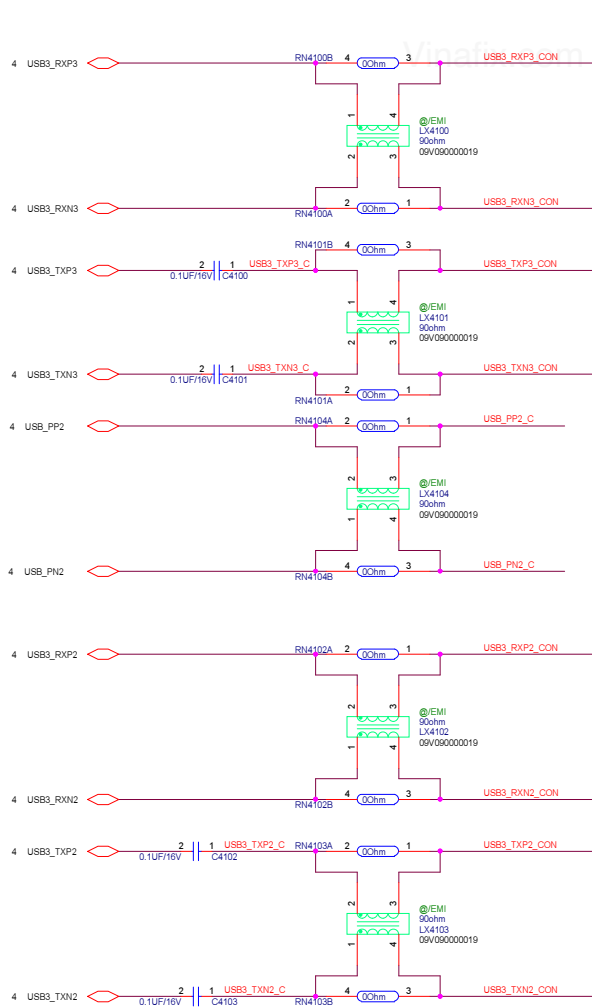
Vinafix.com



<b>PEGATRON</b>		Title : 40. card reader	
BG1/HW3		Engineer: Raly Hsieh	
Size	Project Name		Rev
Custom	AS3EA		2.0
Date: Monday, March 27, 2017		Sheet	40 of 100



# USB3.1 Type C TPS25810



near connector

Vinafix.com



<Variant Name>

<b>PEGATRON</b>		Title <b>USB Type-C Receptacle</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
Engineer: <b>Raly Hsieh</b>			
Size Custom	Project Name <b>AS3EA</b>	Rev 2.0	
Date <b>Monday, March 27, 2017</b>	Sheet <b>42</b> of <b>100</b>		

Hardware Solution For Dead Battery

For notebook applications, if the battery charger needs higher voltage than 5V to operate correctly, execute the steps below in the order they are listed:

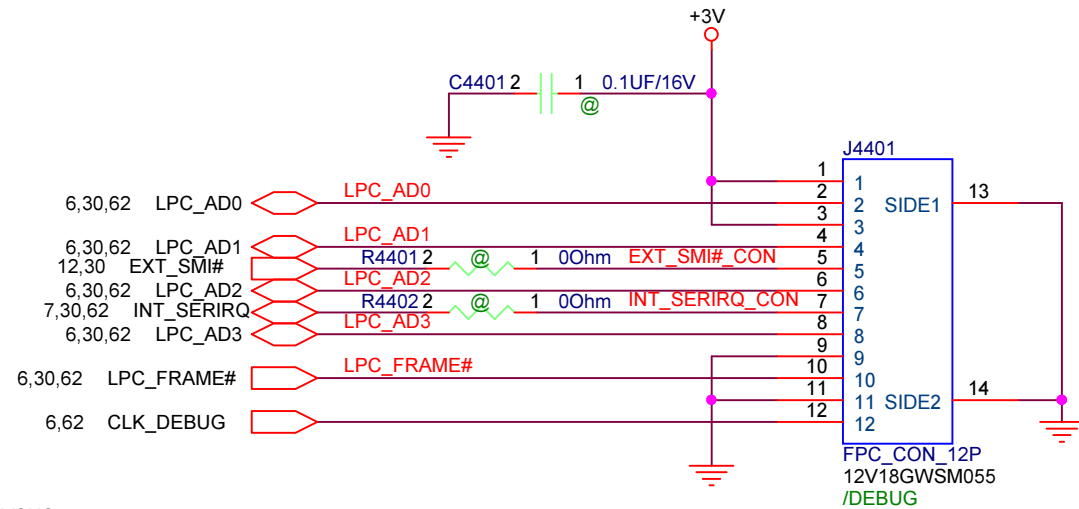
Vinafix.com



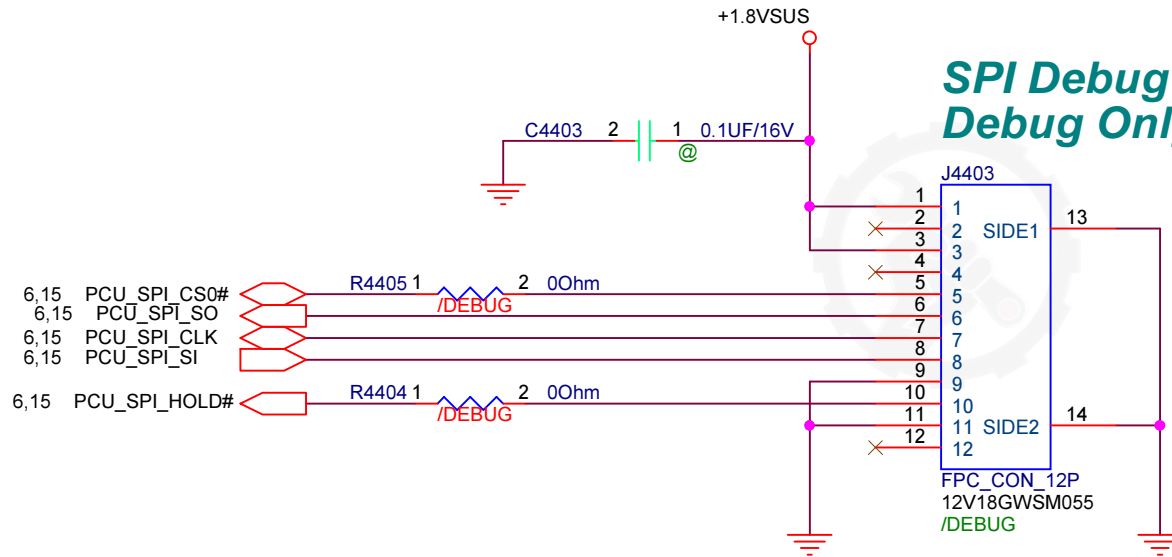
<Variant Name>

<b>PEGATRON</b>		Title : <b>Dead Battery</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
		Engineer: <b>Raly Hsieh</b>	
Size Custom	Project Name <b>AS3EA</b>		Rev 2.0
Date: <b>Monday, March 27, 2017</b>		Sheet <b>43</b> of <b>100</b>	

Vinafix.com



## SPI Debug Port Debug Only



<Variant Name>

**PEGATRON** Title : **BUG\_Debug**  
PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: **Raly Hsieh**

BG1-HW3

Size

Project Name

Rev

Custom

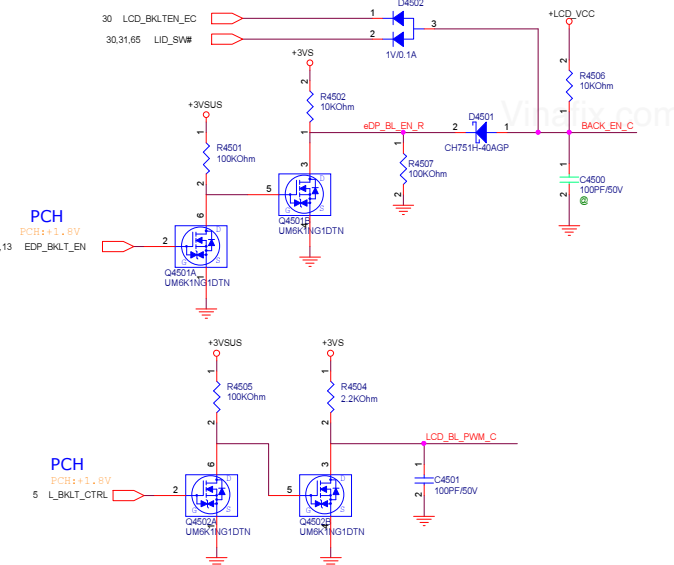
**AS3EA**

2.0

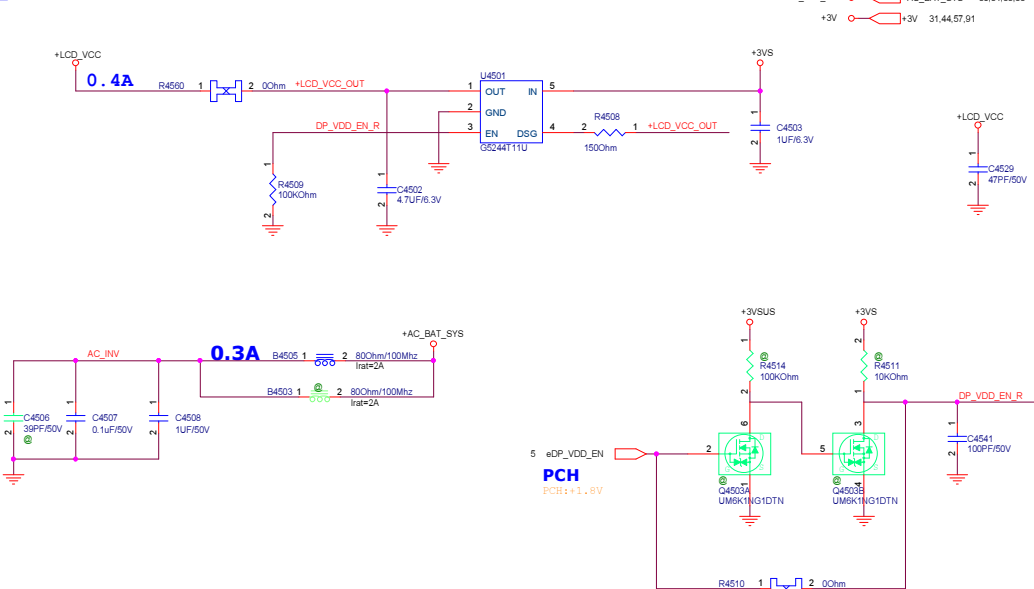
Date: **Monday, March 27, 2017**

Sheet **44** of **100**

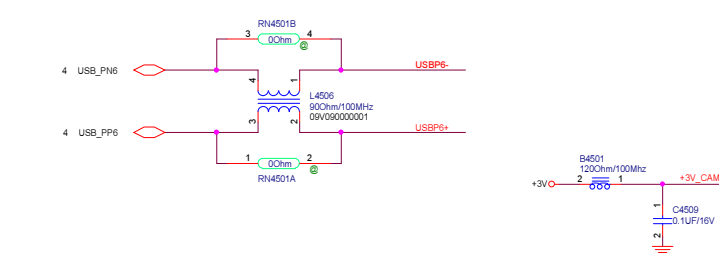
## Controller circuit



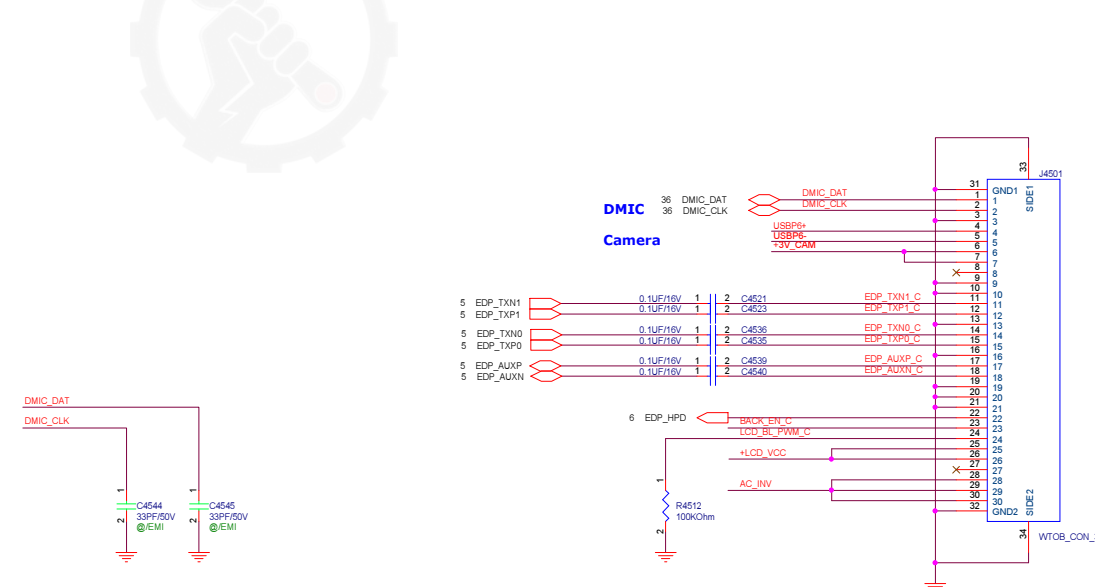
## LCD VCC for eDP



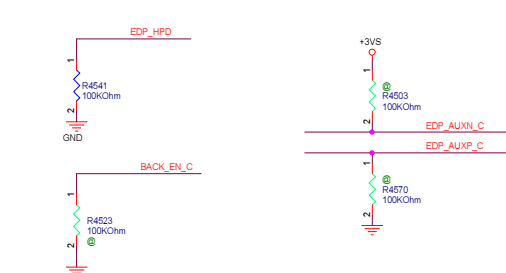
## Camera



### eDP Connector



**eDP HPD**



<Variant Name>

PEGATRON Title : eDP\_output  
PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: **Raly Hsieh**

Size	Project Name	Rev
C	AS3EA	2.0
Date:	Monday, March 27, 2017	Sheet 45 of 100

Vinafix.com



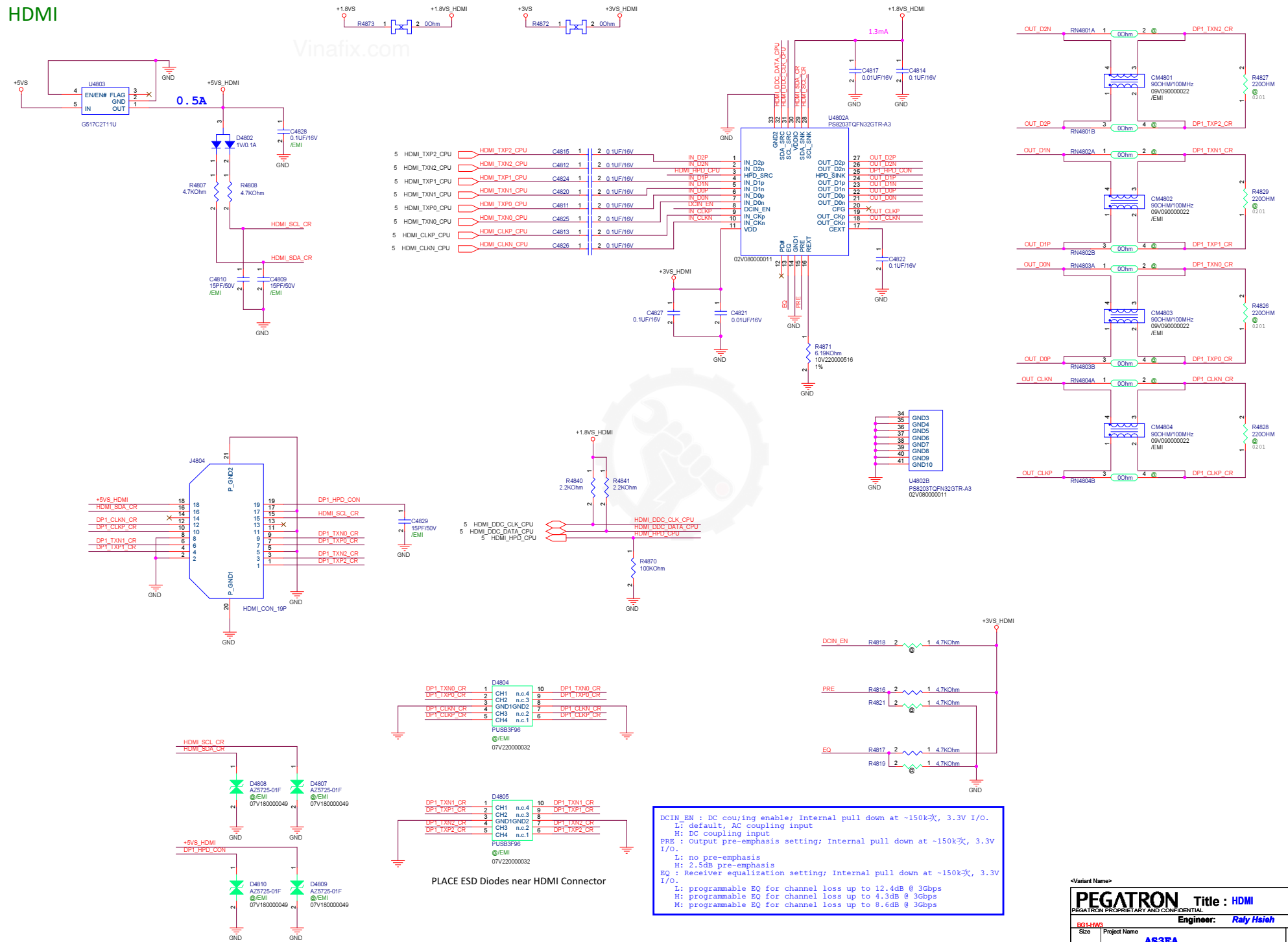
<Variant Name>			
<b>PEGATRON</b>		<b>Title :</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		<b>Engineer:</b>	
Size C	Project Name AS3EA	Rev 2.0	
Date: Monday, March 27, 2017		Sheet	46 of 100

Vinafix.com



<Variant Name>			
<b>PEGATRON</b>		<b>Title :</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		<b>Engineer:</b>	
Size C	Project Name AS3EA	Rev 2.0	
Date: Monday, March 27, 2017		Sheet	47 of 100

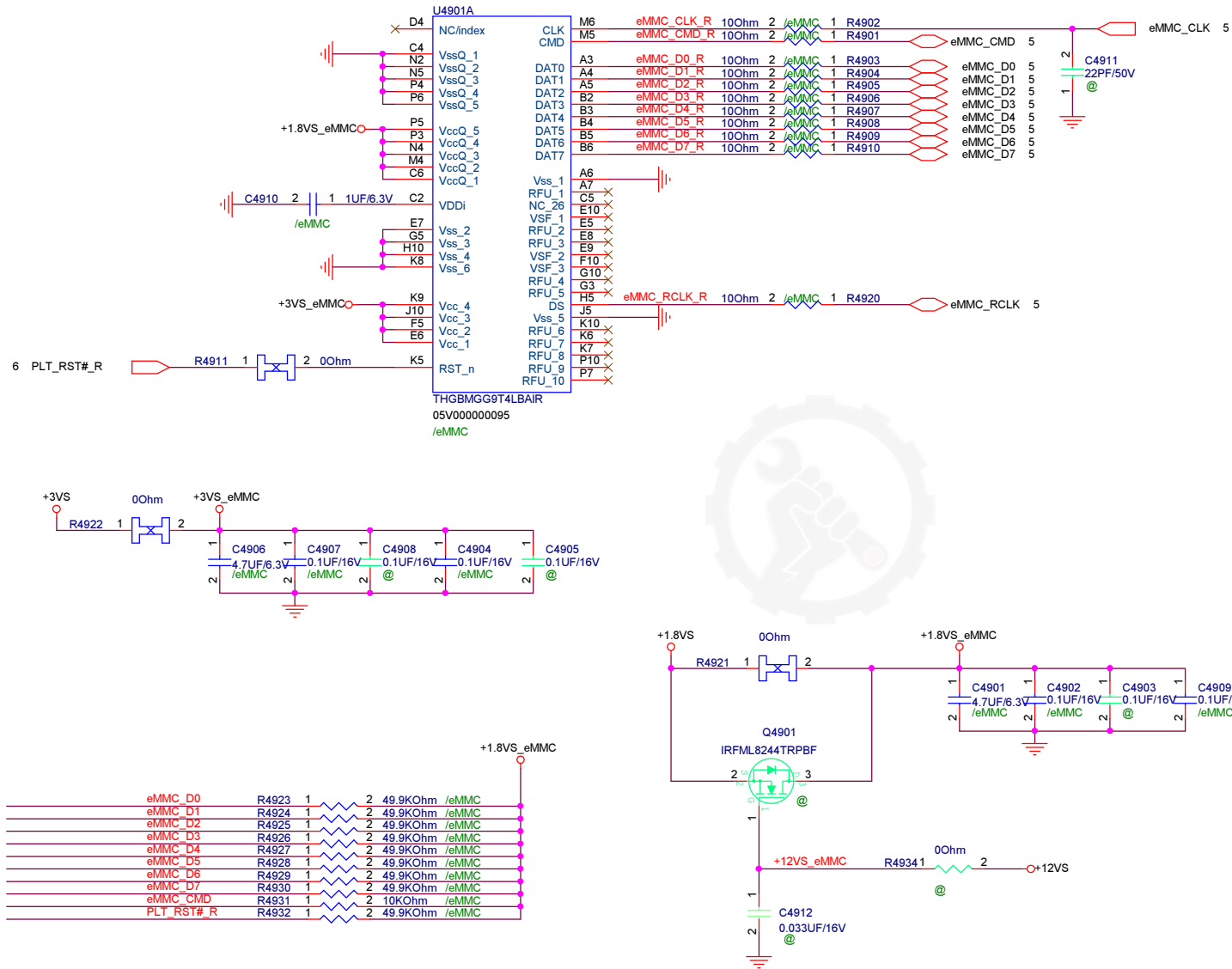
## HDMI





# 49 EMMC

Vinafix.com



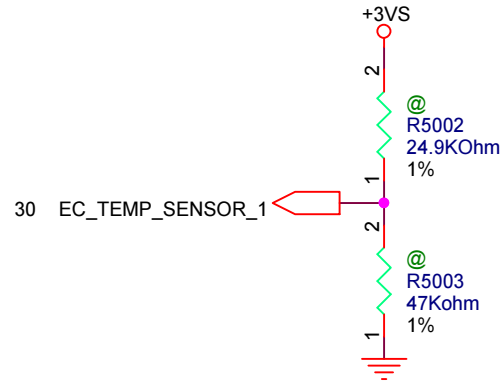
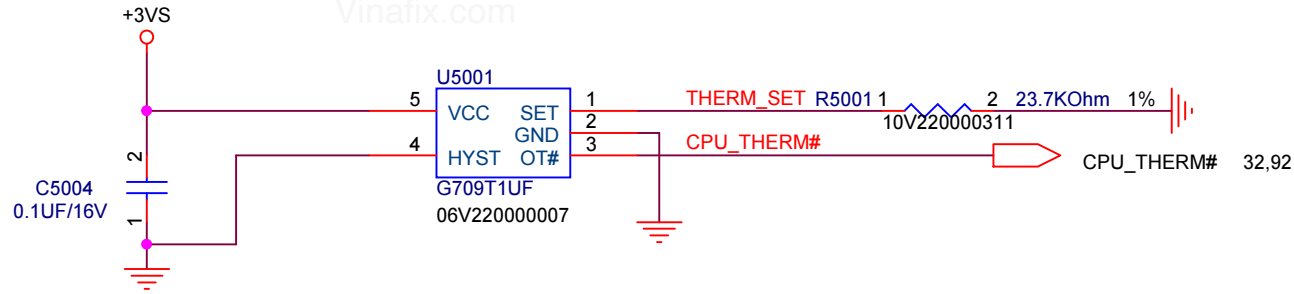
A1	NC_1	NC_54	H12
A10	NC_2	NC_55	H13
A11	NC_3	NC_56	H14
A12	NC_4	NC_57	H2
A13	NC_5	NC_58	H3
A14	NC_6	NC_59	J1
A2	NC_7	NC_60	J12
A8	NC_8	NC_61	J13
A9	NC_9	NC_62	J2
B1	NC_10	NC_63	J3
B10	NC_11	NC_64	K1
B11	NC_12	NC_65	K12
B12	NC_13	NC_66	K13
B13	NC_14	NC_67	K14
B14	NC_15	NC_68	K2
B7	NC_16	NC_69	K3
B8	NC_17	NC_70	L1
B9	NC_18	NC_71	L12
C1	NC_19	NC_72	L13
C10	NC_20	NC_73	L14
C11	NC_21	NC_74	L2
C12	NC_22	NC_75	L3
C13	NC_23	NC_76	M1
C14	NC_24	NC_77	M10
C3	NC_25	NC_78	M11
C7	NC_26	NC_79	M12
C8	NC_27	NC_80	M13
C9	NC_28	NC_81	M14
D1	NC_29	NC_82	M2
D12	NC_30	NC_83	M3
D13	NC_31	NC_84	M7
D14	NC_32	NC_85	M8
D2	NC_33	NC_86	M9
D3	NC_34	NC_87	N1
E1	NC_35	NC_88	N10
E12	NC_36	NC_89	N11
E13	NC_37	NC_90	N12
E14	NC_38	NC_91	N13
E2	NC_39	NC_92	N14
E3	NC_40	NC_93	N3
F1	NC_41	NC_94	N6
F12	NC_42	NC_95	N7
F13	NC_43	NC_96	N8
F14	NC_44	NC_97	N9
F2	NC_45	NC_98	P1
F3	NC_46	NC_99	P11
G1	NC_47	NC_100	P12
G12	NC_48	NC_101	P13
G13	NC_49	NC_102	P14
G14	NC_50	NC_103	P2
G2	NC_51	NC_104	P8
H1	NC_52	NC_105	P9
H12	NC_53	NC_106	

THGBMG9T4LBAIR  
05V000000095  
/eMMC

<Variant Name>

<b>PEGATRON</b>		Title : <b>eMMC</b>	
BG1-HW3		Engineer: <b>Raly Hsieh</b>	
Size Custom	Project Name <b>AS3EA</b>		Rev 2.0
Date: <b>Monday, March 27, 2017</b>	Sheet <b>49</b>	of <b>100</b>	

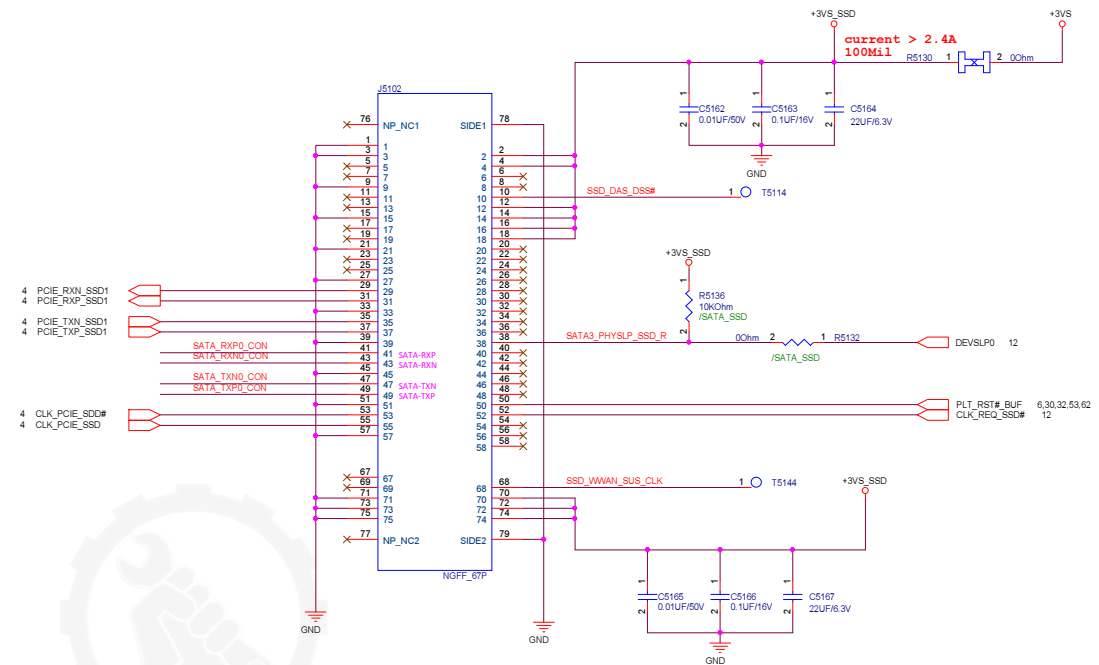
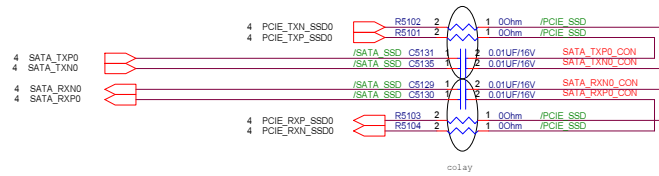
+3VS +3VS 6,12,30,31,32,36,37,41,45,48,49,51,53,57,62,66,91,92  
+5VS +5VS 31,36,48,57,69,91



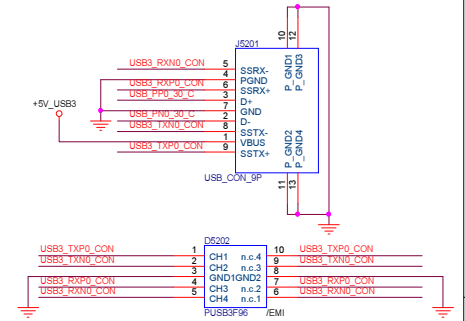
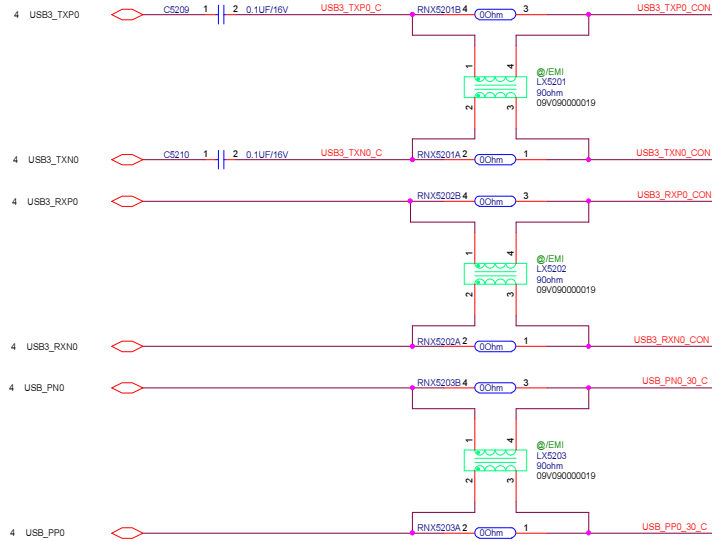
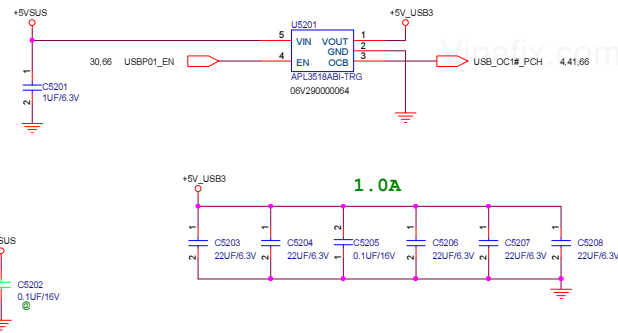
<b>PEGATRON</b>		Title : <b>THERMAL</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG1-HW3</b>		Engineer: <b>Raly Hsieh</b>	
Size	Project Name		Rev
<b>Custom</b>	<b>AS3EA</b>		<b>2.0</b>
Date: <b>Monday, March 27, 2017</b>	Sheet	<b>50</b>	of <b>100</b>

### SATA SSD NGFF socket (M-key)

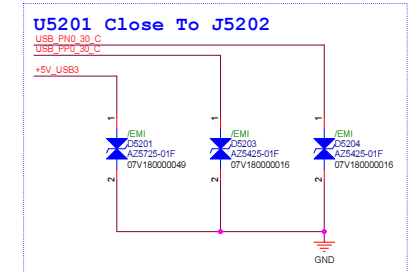
+3VS  +3VS 6, 12, 30, 31, 32, 36, 37, 41, 45, 48, 49, 50, 53, 57, 62, 66, 91, 92  
+5VS  +5VS 31, 36, 48, 57, 69, 91



# 52 USB3.0 Port 0

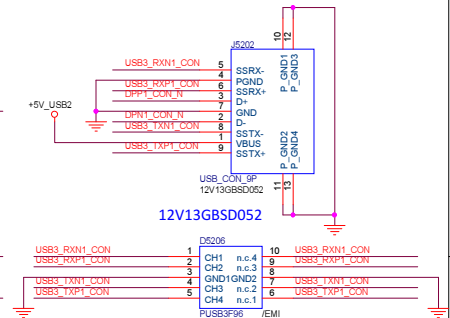
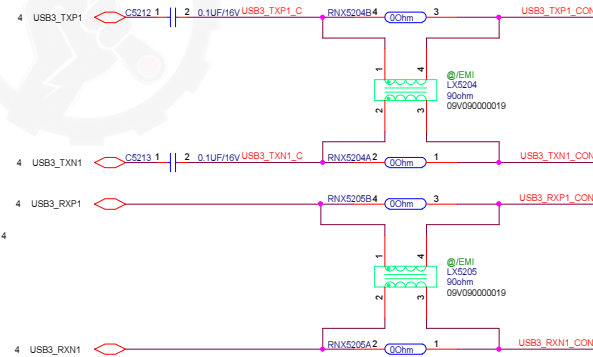
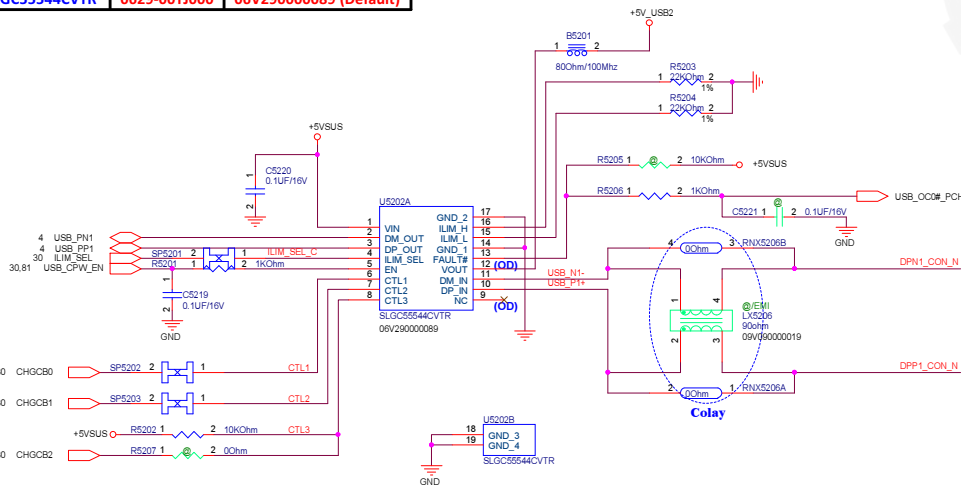


PLACE ESD Diodes near USB Connector

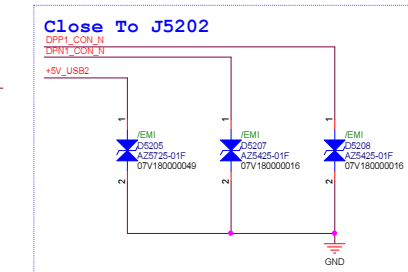


# USB3.0 Port 1 S&C

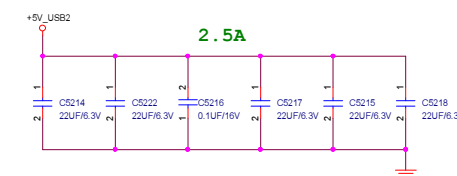
Device	Pega No.	VX No.
SLGC55544CVTR	0629-00TJ000	06V290000089 (Default)



PLACE ESD Diodes near USB Connector



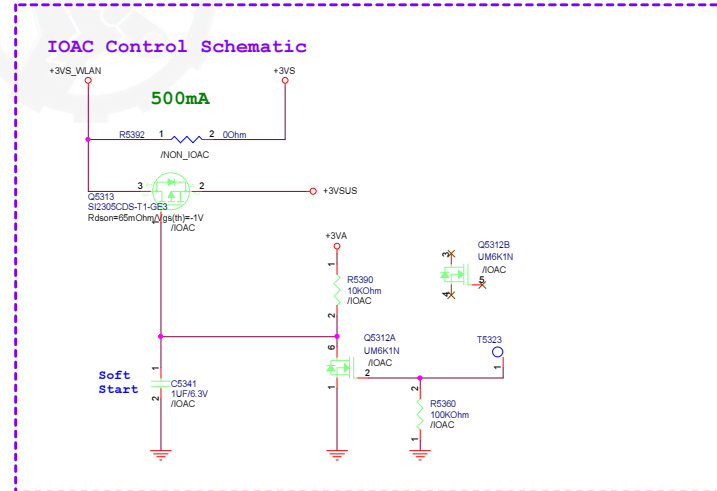
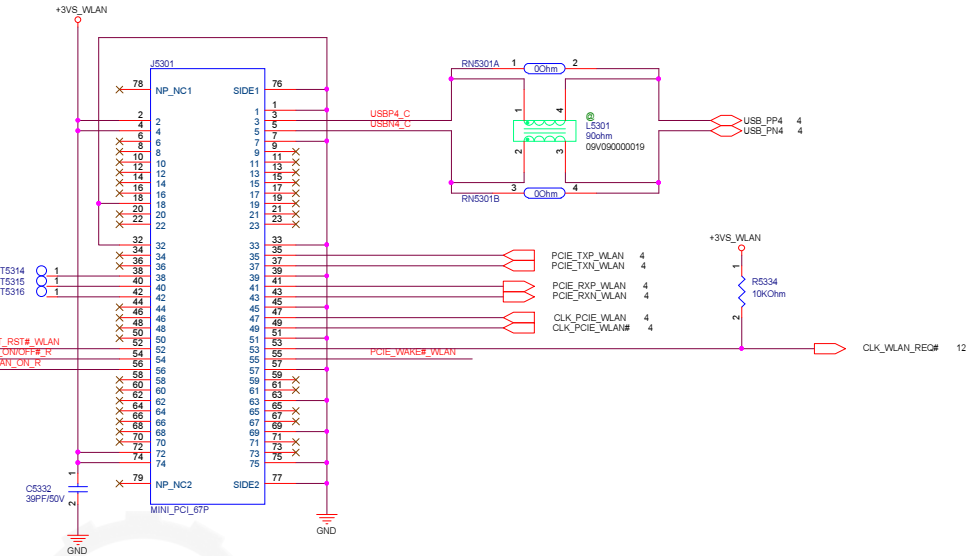
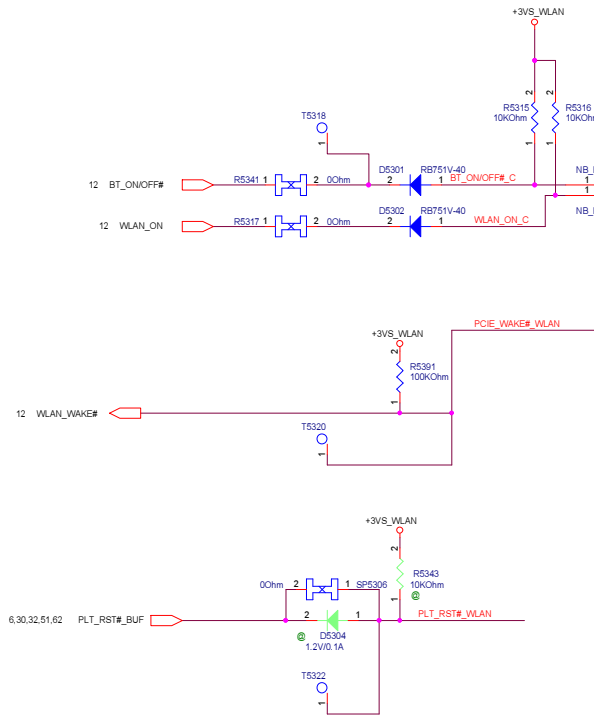
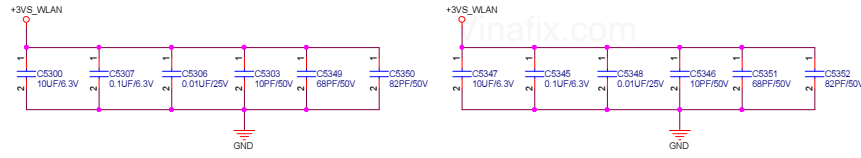
System Global Power State	TPS2544 Charging Mode	CTL1	CTL2	CTL3	ILIM_SEL	Current Limit Setting
S0	SDP (Standard Downstream)	1	1	0	1 or 0	ILIM_HI / ILIM_LO
S0	SDP, no discharge to / from CDP	1	1	1	0	ILIM_LO
S0	CDP, if a BCL2 primary detection occurs	1	1	1	1	ILIM_HI
S3/S4/S5	Auto mode, no mouse wake	0	0	1	0	ILIM_HI
S3	Dedicated Charging Port Auto mode, keyboard/mouse wake up	0	1	1	X	ILIM_HI
S3	SDP, keyboard/mouse wake-up	0	1	0	1 or 0	ILIM_HI / ILIM_LO



+3V\_WLAN\_WP1 bypass capacitor:

+3V\_WLAN\_WP1 bypass capacitor:

# WLAN / BT



Vinafix.com



<b>PEGATRON</b>		<b>Title :</b> USB_HUB	
BG1-HW3 RD		<b>Engineer:</b> Raly Hsieh	
Size	Project Name		Rev
Custom	AS3EA		2.0
Date: Monday, March 27, 2017		Sheet 54 of 100	

Vinafix.com



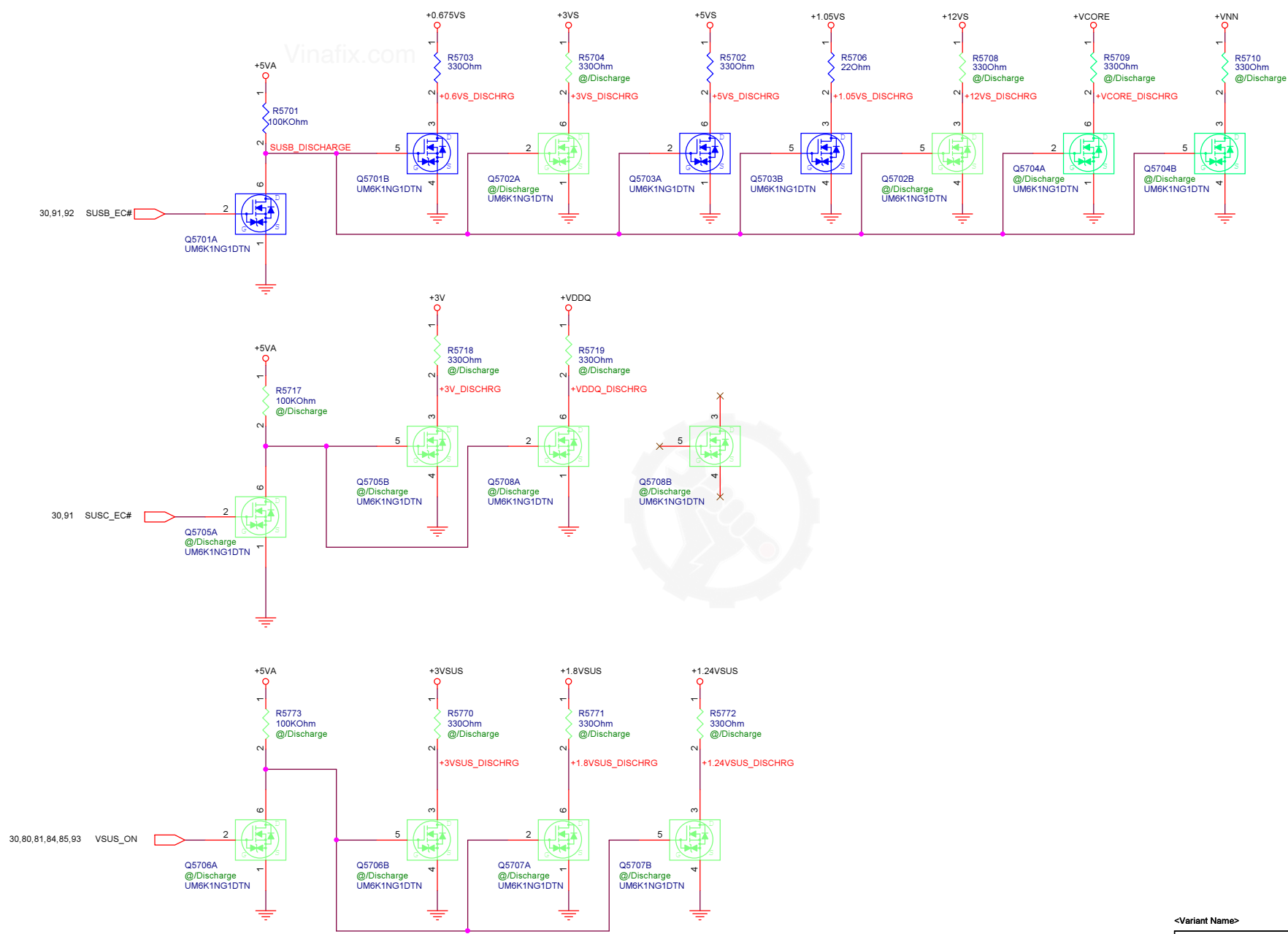
<b>PEGATRON</b>		<b>Title:</b> <i>SATA SSD_HDD</i>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<i>BGT-NB4</i>		<b>Engineer:</b> <i>Raly Hsieh</i>	
Size	Project Name	Rev	
<i>C</i>	<i>AS3EA</i>	<i>2.0</i>	
Date: <i>Monday, March 27, 2017</i>		Sheet	<i>55</i> of <i>100</i>

Vinafix.com



<b>PEGATRON</b>		Title : <b>LED</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG1/HW3</b>		Engineer: <b>Raly Hsieh</b>	
Size	Project Name		Rev
Custom	<b>AS3EA</b>		<b>2.0</b>
Date: <b>Monday, March 27, 2017</b>		Sheet <b>56</b> of <b>100</b>	





<Variant Name>

<b>PEGATRON</b>		<b>Title : Discharge</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1-HW3		Engineer: Raly Hsieh	
Size	Project Name	Rev	
Custom	AS3EA	2.0	
Date: Monday, March 27, 2017		Sheet	57 of 100

Vinafix.com

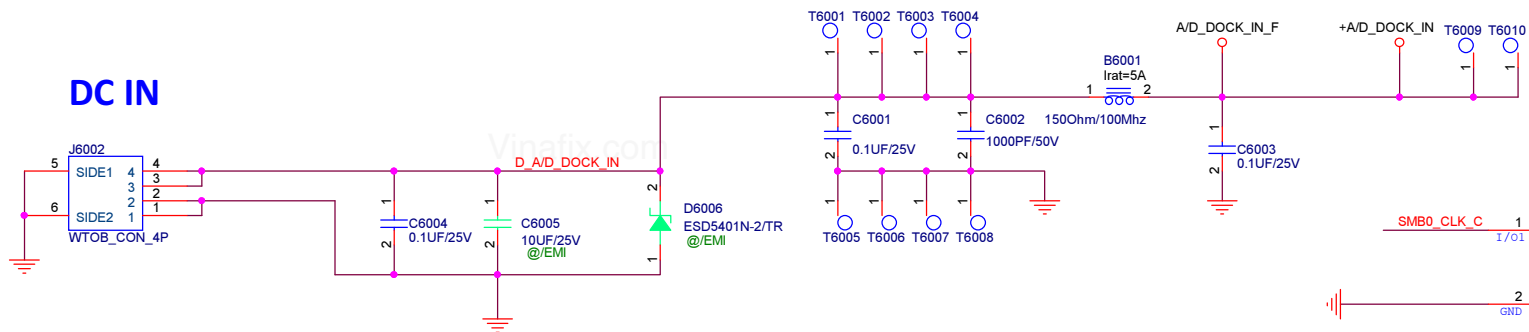


<b>PEGATRON</b>		<b>Title : ASM1042</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1-HW RD Center-HW RD Div.2-HW RD		Engineer: <b>Raly Hsieh</b>	
Size C	Project Name <b>AS3EA</b>		Rev 2.0
Date: Monday, March 27, 2017		Sheet	56 of 100

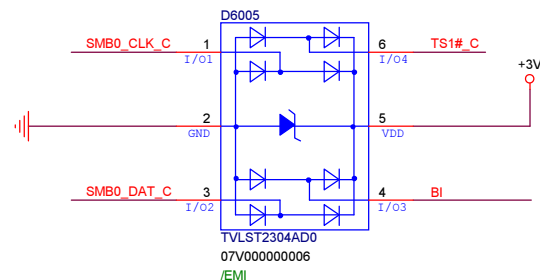
Vinafix.com



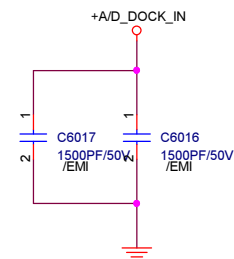
## DC IN



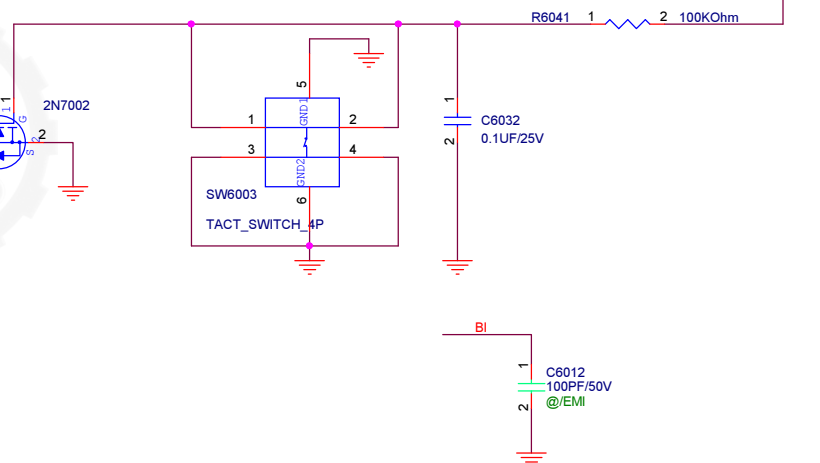
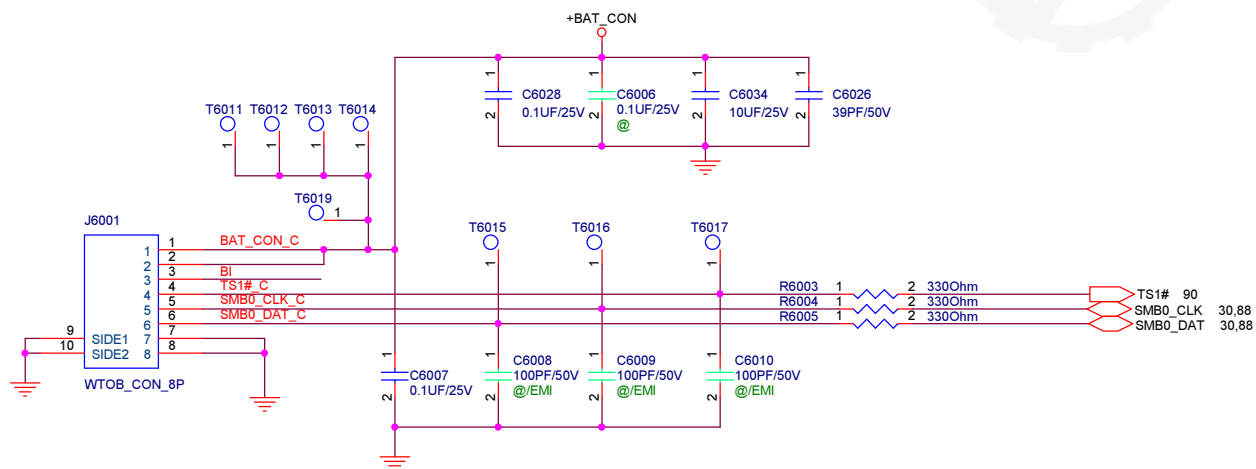
+BAT\_CON 88  
+3VA 9,30,31,36,53,65,81,88,93  
+A/D\_DOCK\_IN 88



## EMI



## Battery Connector



**PEGATRON** Title : DC-IN/ Batt connector  
PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW3 Engineer: Raly Hsieh  
Size Project Name AS3EA Rev 2.0  
Custom Date: Monday, March 27, 2017 Sheet 60 of 100

Vinafix.com



<Variant Name>

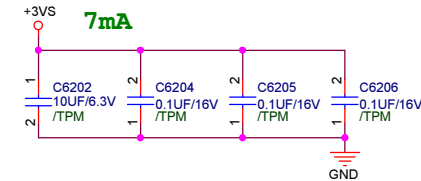
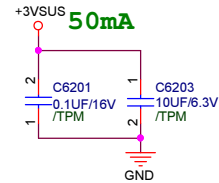
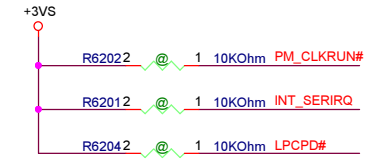
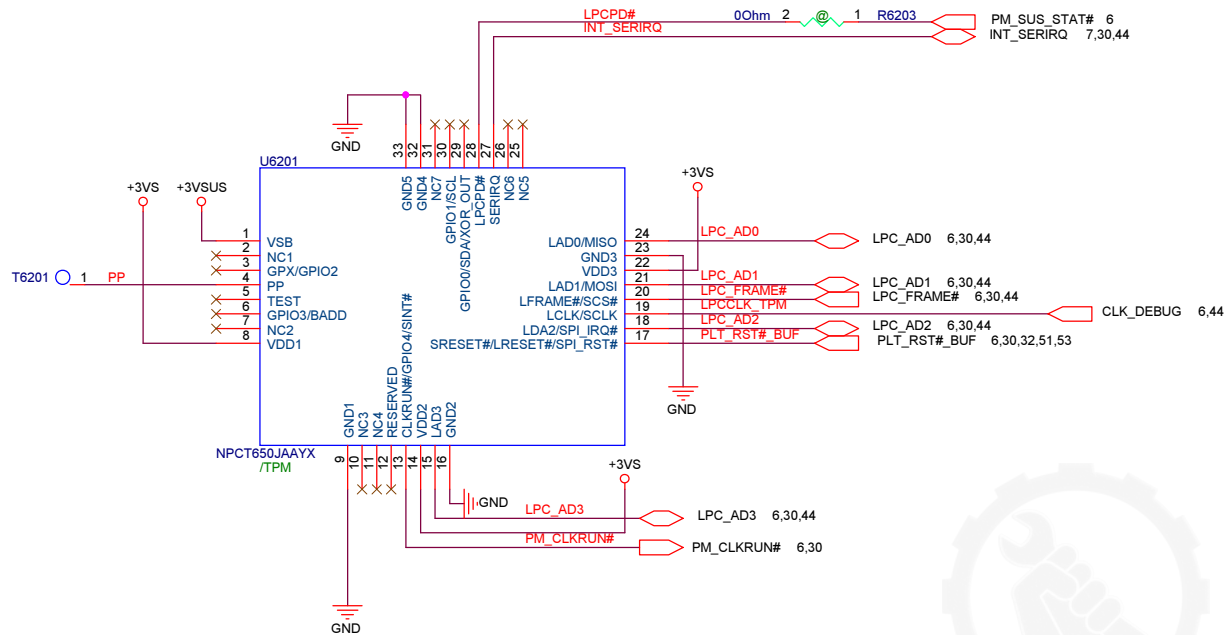
**PEGATRON** Title : Touch Panel Conn  
PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3 Engineer: Raly Hsieh

Size Custom	Project Name	Rev 2.0
----------------	--------------	------------

Date: Monday, March 27, 2017 Sheet 61 of 100

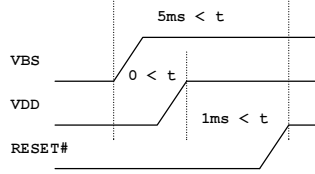
Vinafix.com



## TPM

VDD: Power the I/O buffers of the GPIO ports and the Host Interface  
VSB: Standby 3.3V Power Supply. Powers the on-chip Core.

### TPM Power Sequence



NOTE: RESET# is LRESET#, SPI\_RST# or SRESET#.

#### NOTE:

- 1) For TPM 1.2:  
The TPM VSB pin must be connected to the system's standby voltage (existing at S3 power state).
- 2) For TPM 2.0:  
It is recommended to connect the TPM VSB pin to the system's standby voltage to improve performance.
- 3) TPM VDD pins should be connected to the same power rail that feeds the Chipset LPC interface.
- 4) RESET# must be asserted for at least 5 msec after VSB power-up.
- 5) VSB may come up anytime before VDD power-up, but not after VDD power-up.
- 6) RESET# may be asserted together with VDD power negation, but should not at any point exceed 0.5V above the VDD power level.

**PEGATRON** Title : **TPM NPCT650**

BG1-NB4

Engineer: **Raly Hsieh**

Size	Project Name	Rev
B	AS3EA	2.0

Date: **Monday, March 27, 2017**

Sheet **62** of **100**

Vinafix.com



<Variant Name>			
<b>PEGATRON</b>		<b>Title :</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		<b>Engineer:</b>	
Size C	Project Name AS3EA	Rev 2.0	
Date: Monday, March 27, 2017		Sheet	63 of 100

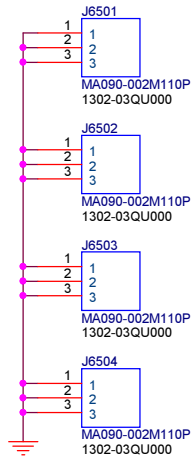
Vinafix.com



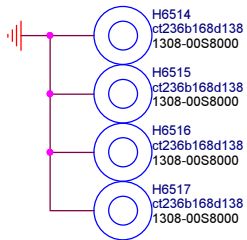
<b>PEGATRON</b>		Title : <b>IO Board</b>	
331-854		Engineer: <b>Raly Hsieh</b>	
Size	Project Name		Rev
C	<b>AS3EA</b>		2.0
Date: <b>Monday, March 27, 2017</b>		Sheet	64 of 100



## CLIP JCT



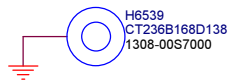
## CPU NUTx4



## WLAN NUT

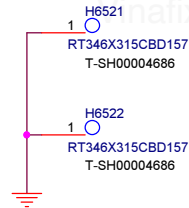


## Thermal NUT

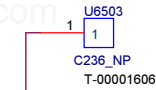


## ME Screw Hole

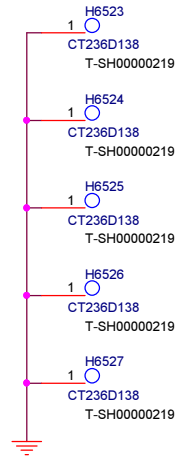
### Screw Hole A



### Screw Hole B



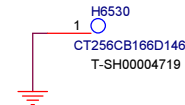
### Screw Hole C



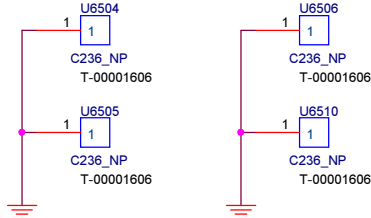
### Screw Hole D



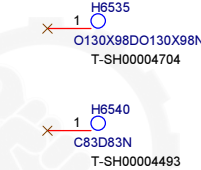
### Screw Hole E



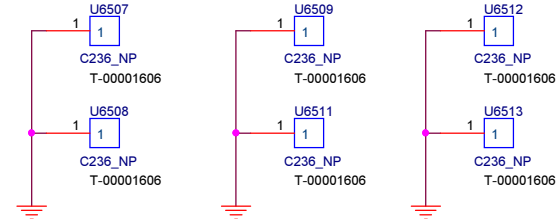
### PAD Top



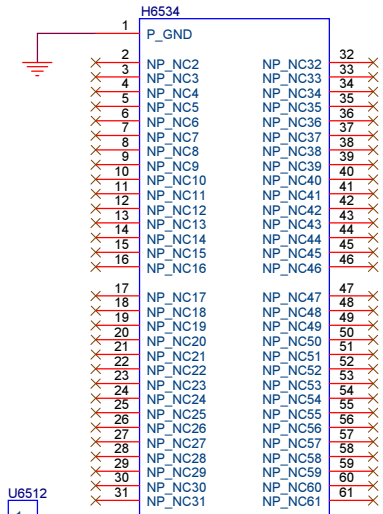
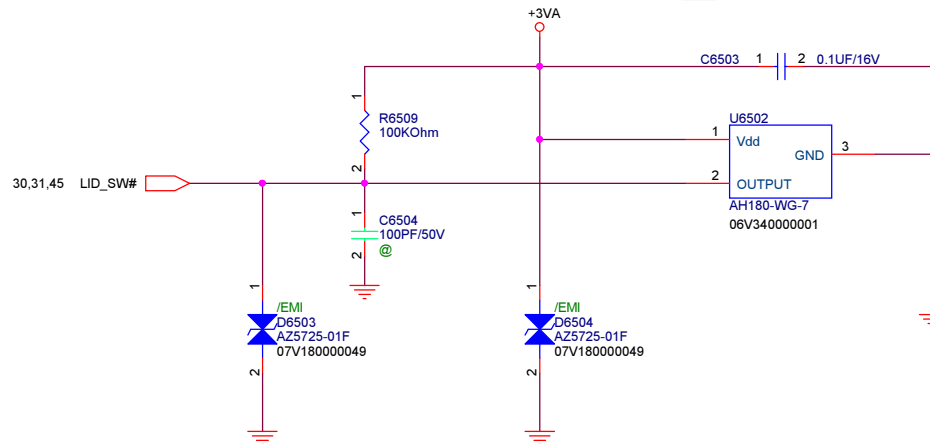
### Tooling Hole



### PAD Bottom



## Hall Sensor



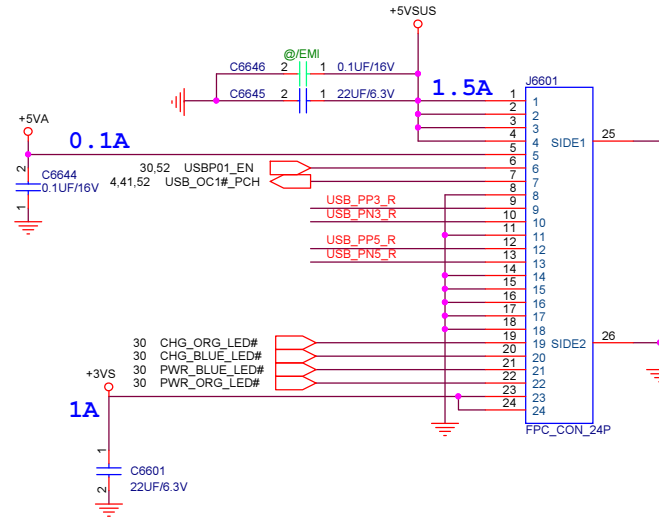
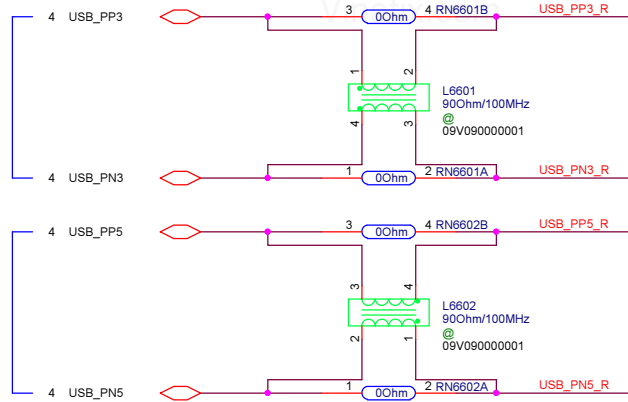
<Variant Name>

<b>PEGATRON</b>		Title : <b>ME_CONN,Skew Hole</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG1-HW3</b>		Engineer: <b>Raly Hsieh</b>	
Size	Project Name		Rev
<b>B</b>	<b>AS3EA</b>		<b>2.0</b>
Date: <b>Monday, March 27, 2017</b>		Sheet	<b>65</b> of <b>100</b>

# DB CONN

USB2.0 (IO)

CR



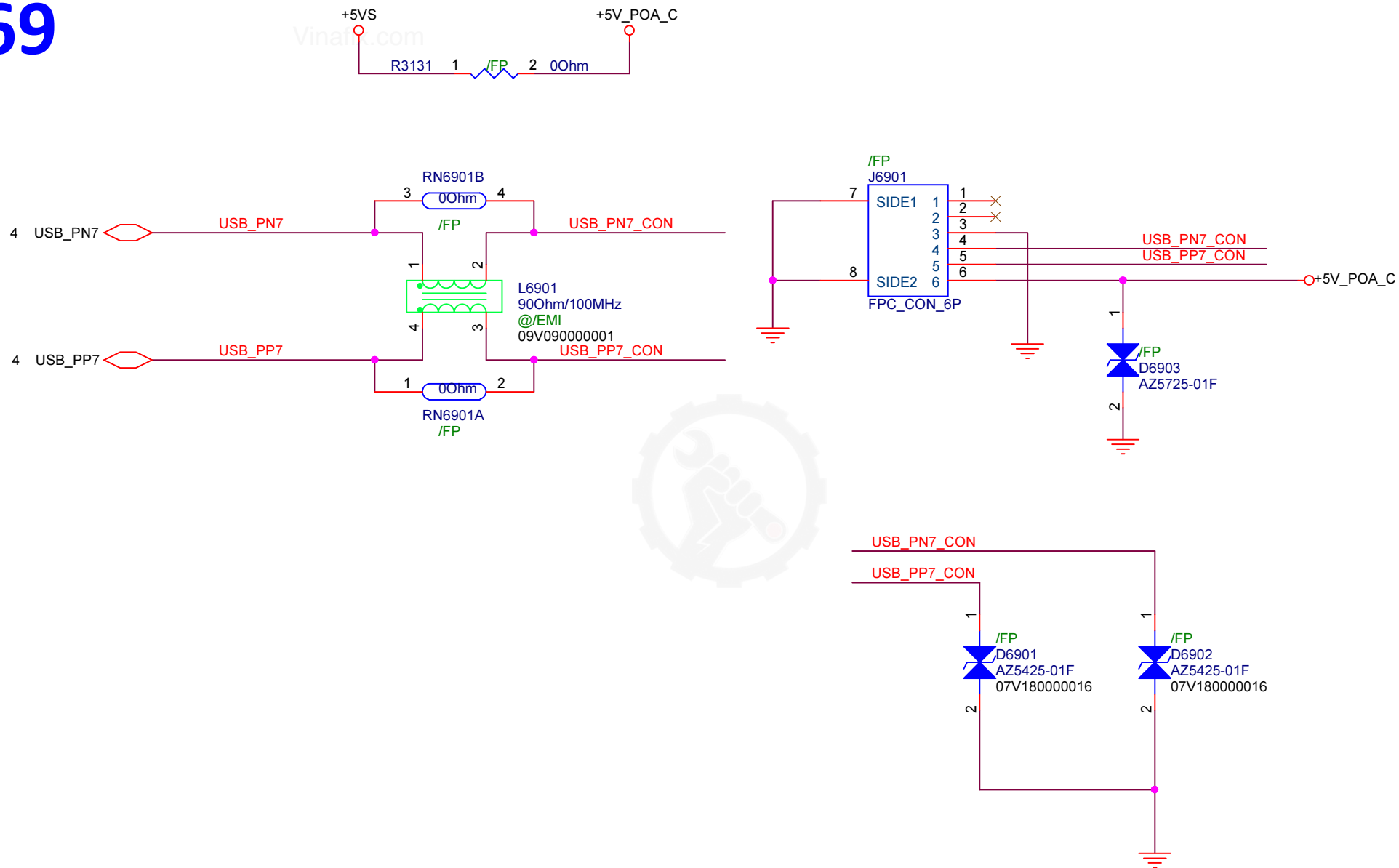
Vinafix.com



Vinafix.com



<Variant Name>			
<b>PEGATRON</b>		<b>Title :</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		<b>Engineer:</b>	
Size C	Project Name AS3EA	Rev 2.0	
Date: Monday, March 27, 2017		Sheet 66 of 100	



Vinafix.com



<b>PEGATRON</b>		Title : 70. *****	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW4		Engineer: Raly Hsieh	
Size A	Project Name AS3EA		Rev 2.0
Date: Monday, March 27, 2017		Sheet 70 of 100	

Vinafix.com



<b>PEGATRON</b>		Title : <b>71. *****</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG1/HW4</b>		Engineer: <b>Raly Hsieh</b>	
Size <b>A</b>	Project Name <b>AS3EA</b>		Rev <b>2.0</b>
Date: <b>Monday, March 27, 2017</b>		Sheet <b>71</b> of <b>100</b>	

Vinafix.com



<b>PEGATRON</b>		Title : 72. *****	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW4		Engineer: Raly Hsieh	
Size A	Project Name AS3EA		Rev 2.0
Date: Monday, March 27, 2017		Sheet 72 of 100	



Vinafix.com



<b>PEGATRON</b>		Title : <b>73. *****</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG1/HW4</b>		Engineer: <b>Raly Hsieh</b>	
Size <b>A</b>	Project Name <b>AS3EA</b>		Rev <b>2.0</b>
Date: <b>Monday, March 27, 2017</b>		Sheet <b>73</b> of <b>100</b>	

Vinafix.com



<b>PEGATRON</b>		Title : <b>74. *****</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG1/HW4</b>		Engineer: <b>Raly Hsieh</b>	
Size <b>A</b>	Project Name <b>AS3EA</b>		Rev <b>2.0</b>
Date: <b>Monday, March 27, 2017</b>		Sheet <b>74</b> of <b>100</b>	

Vinafix.com



<b>PEGATRON</b>		Title : <b>75. *****</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG1/HW4</b>		Engineer: <b>Raly Hsieh</b>	
Size <b>A</b>	Project Name <b>AS3EA</b>		Rev <b>2.0</b>
Date: <b>Monday, March 27, 2017</b>		Sheet <b>75</b> of <b>100</b>	

Vinafix.com



<b>PEGATRON</b>		Title : <b>76. *****</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG1/HW4</b>		Engineer: <b>Raly Hsieh</b>	
Size <b>A</b>	Project Name <b>AS3EA</b>		Rev <b>2.0</b>
Date: <b>Monday, March 27, 2017</b>		Sheet <b>76</b> of <b>100</b>	

Vinafix.com



<b>PEGATRON</b>		Title : <b>77.*****</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG1/HW4</b>		Engineer: <b>Raly Hsieh</b>	
Size <b>A</b>	Project Name <b>AS3EA</b>		Rev <b>2.0</b>
Date: <b>Monday, March 27, 2017</b>		Sheet <b>77</b> of <b>100</b>	

Vinafix.com

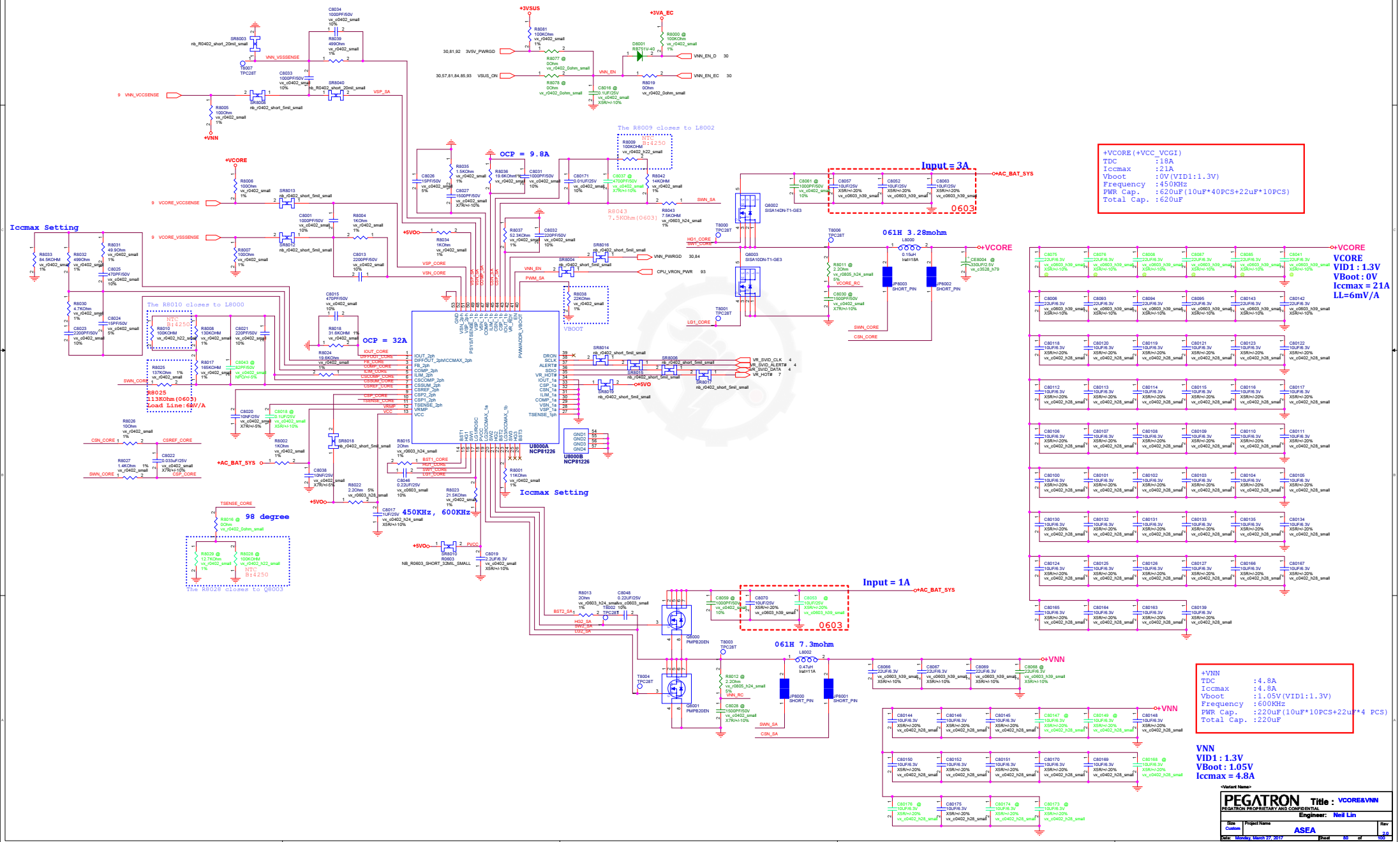


<b>PEGATRON</b>		Title : <b>78. *****</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG1/HW4</b>		Engineer: <b>Raly Hsieh</b>	
Size <b>A</b>	Project Name <b>AS3EA</b>		Rev <b>2.0</b>
Date: <b>Monday, March 27, 2017</b>		Sheet <b>78</b> of <b>100</b>	

Vinafix.com



<b>PEGATRON</b>		Title : <b>79. *****</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG1/HW4</b>		Engineer: <b>Raly Hsieh</b>	
Size <b>A</b>	Project Name <b>AS3EA</b>		Rev <b>2.0</b>
Date: <b>Monday, March 27, 2017</b>		Sheet <b>79</b> of <b>100</b>	





Vinafix.com



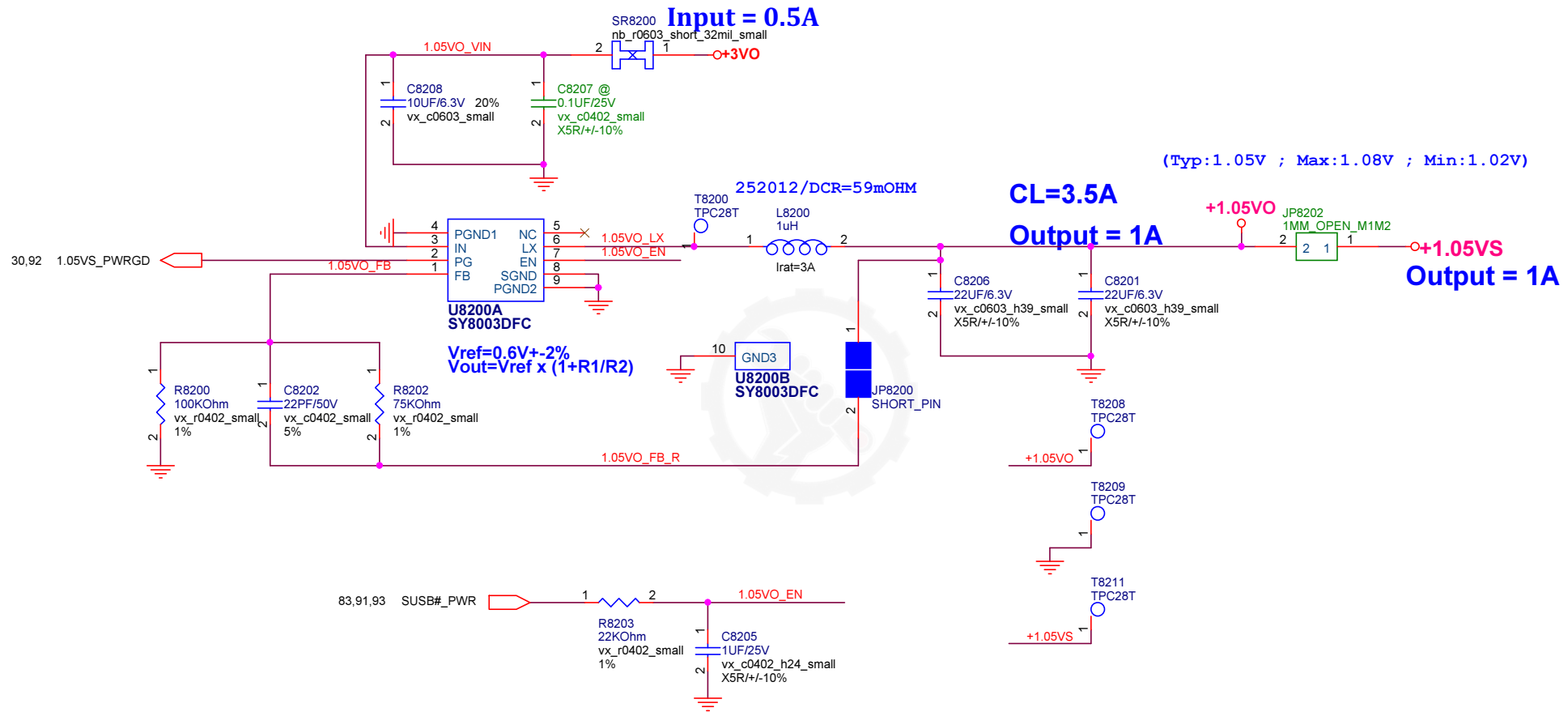
PEGATRON PROPRIETARY AND CONFIDENTIAL

---

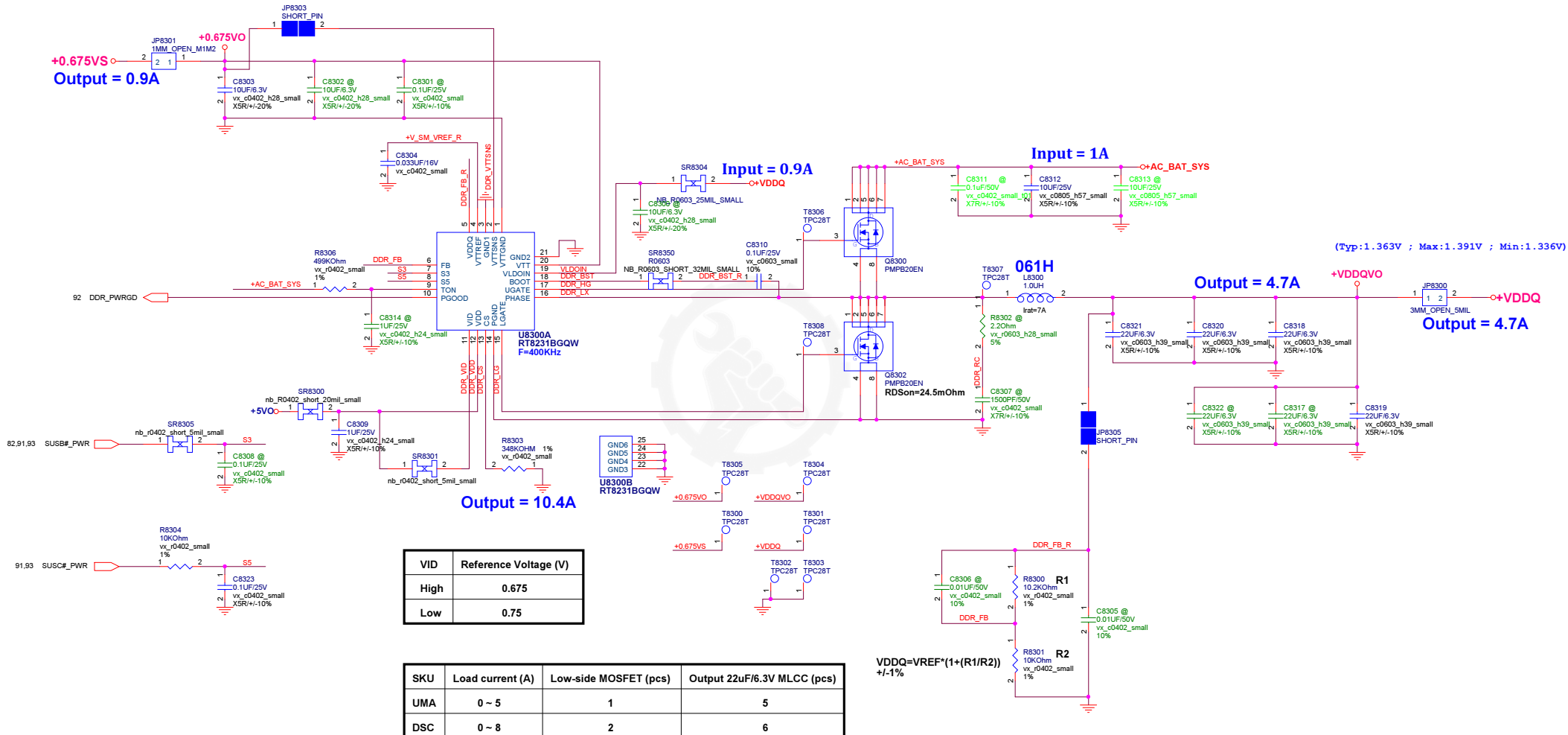
Custom AS3EA

---

# +1.05VO POWER SUPPLY



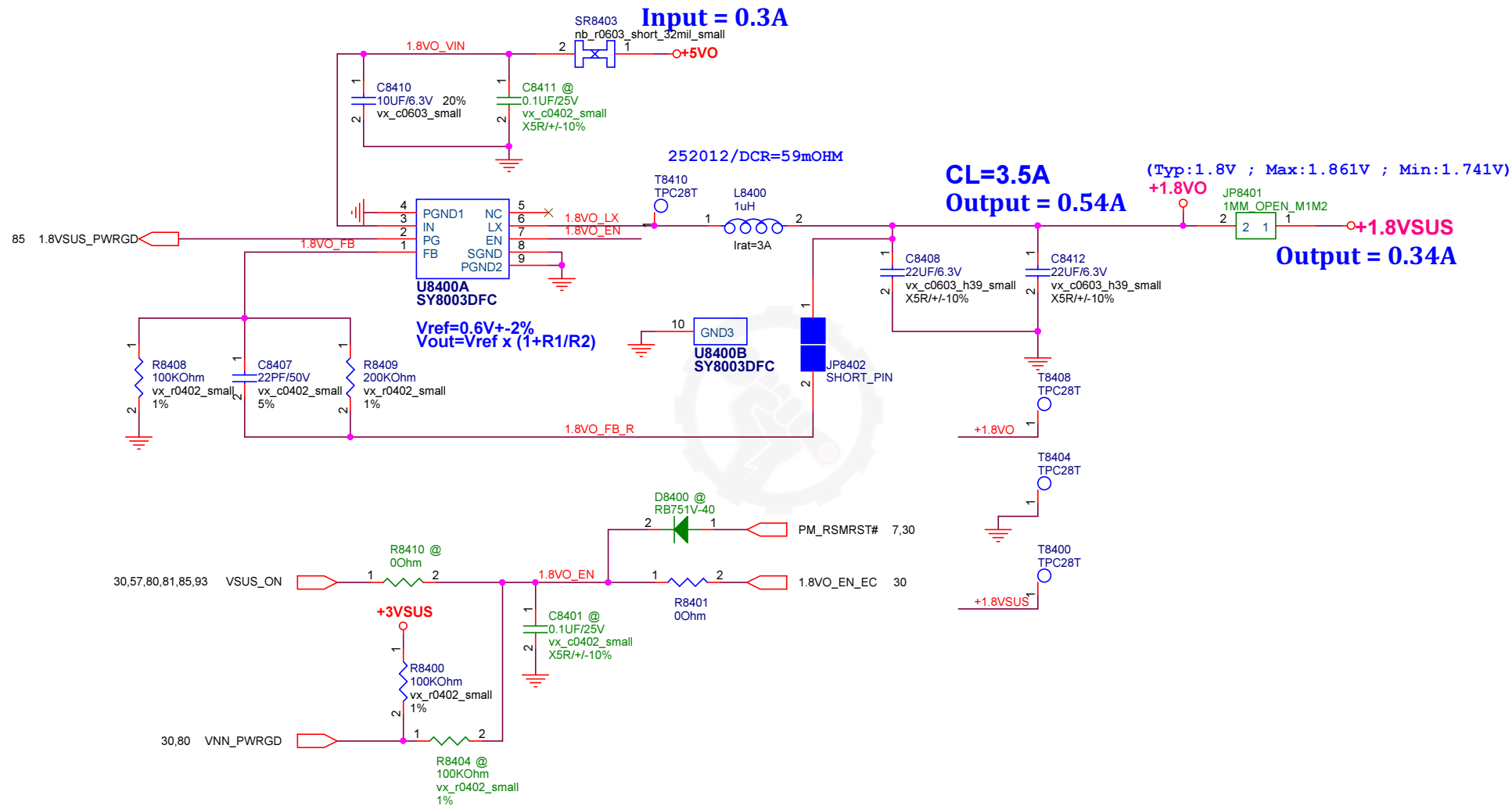
## DDR & VTT POWER SUPPLY



VID	Reference Voltage (V)
High	0.675
Low	0.75

SKU	Load current (A)	Low-side MOSFET (pcs)	Output 22uF/6.3V MLCC (pcs)
UMA	0 ~ 5	1	5
DSC	0 ~ 8	2	6

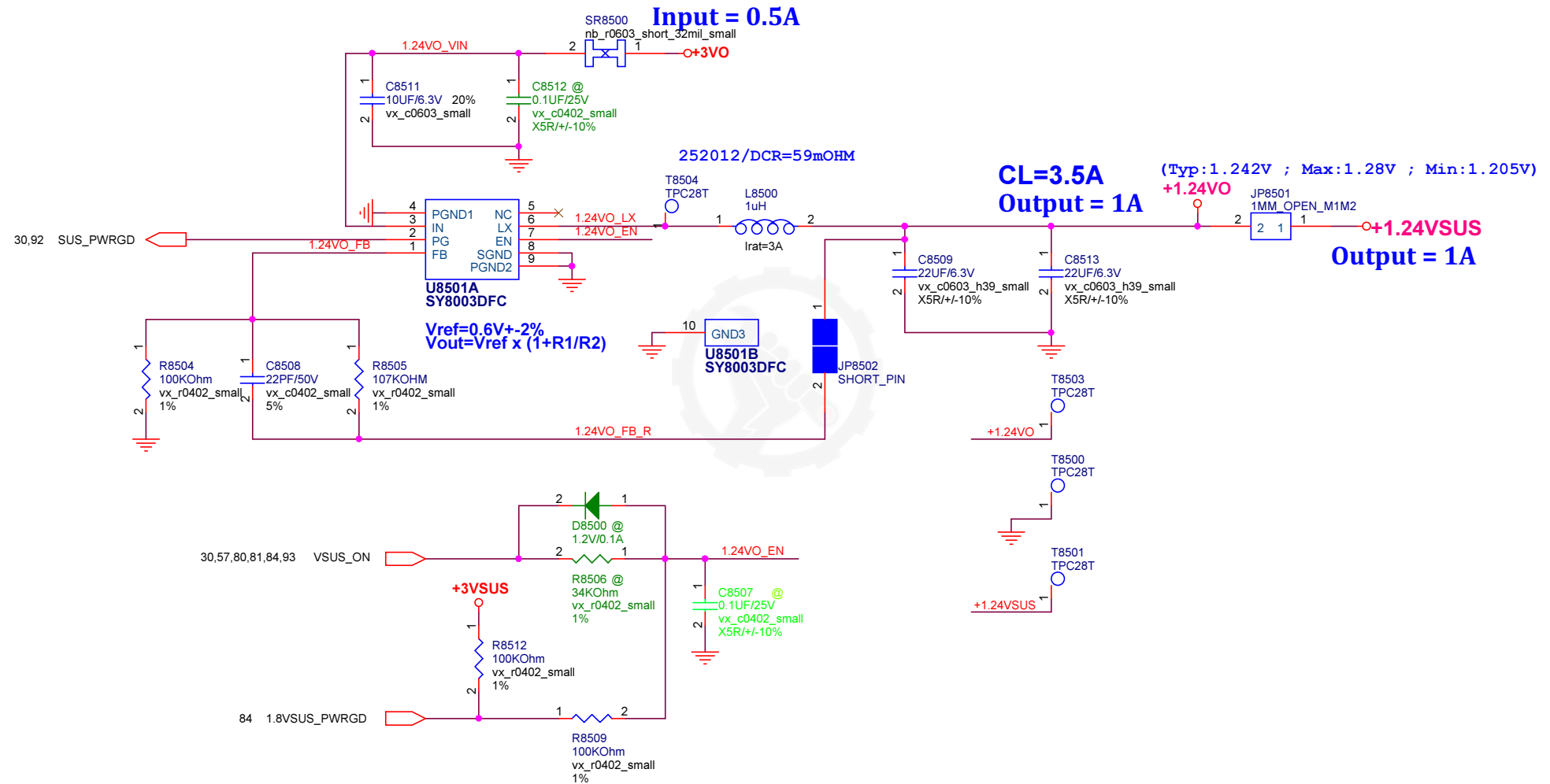
# Vinafix.com +1.8VO POWER SUPPLY



<Variant Name>

<b>PEGATRON</b>		<b>Title :</b>	<b>1.8VSUS</b>
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>Engineer:</b>		<b>Neil Lin</b>	
Size Custom	Project Name	<b>TJ13A</b>	
Date:	Monday, March 27, 2017	Sheet	84 of 100
		Rev	<b>2.0</b>

# +1.24VO POWER SUPPLY

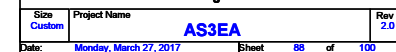


&lt;Variant Name&gt;

**PEGATRON** Title : **1.24VSUS**  
PEGATRON PROPRIETARY AND CONFIDENTIAL

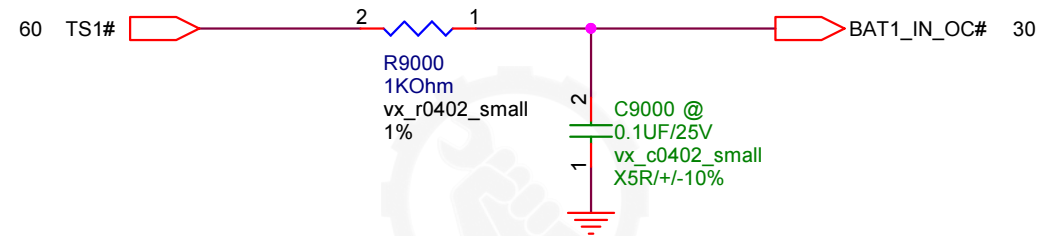
Engineer: **Neil Lin**

Size Custom	Project Name <b>AS3EA</b>	Rev <b>2.0</b>
Date: <b>Monday, March 27, 2017</b>	Sheet <b>85</b> of <b>100</b>	



Add 0609-00AK000 for avoiding shortage

## BATTERY IN DETECT

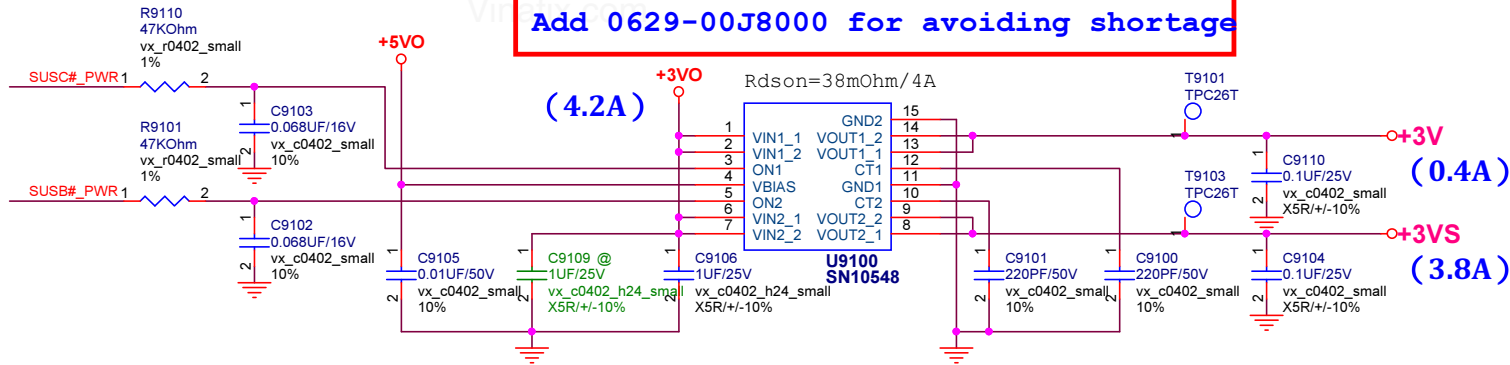


<Variant Name>

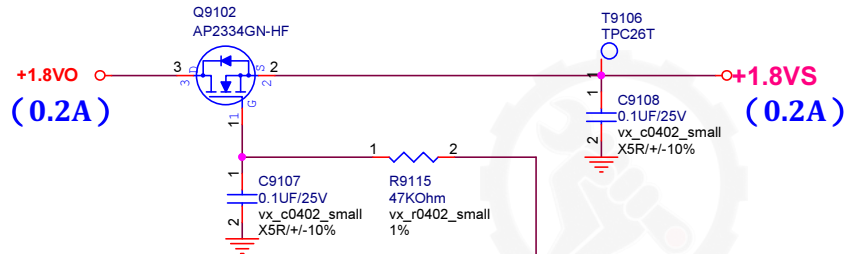
<b>PEGATRON</b>		Title : <b>DETECT</b>
PEGATRON PROPRIETARY AND CONFIDENTIAL		
Engineer: <b>Neil Lin</b>		
Size Custom	Project Name <b>AS3EA</b>	Rev 2.0
Date: <b>Monday, March 27, 2017</b>	Sheet <b>90</b> of <b>100</b>	

# SUSB# & SUSC# POWER

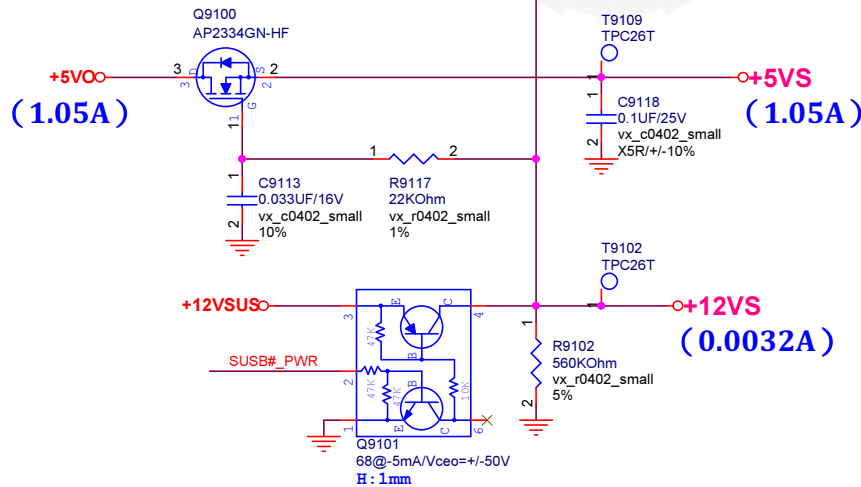
Add 0629-00J8000 for avoiding shortage



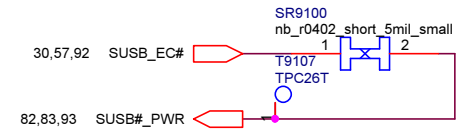
VGS=10V, RDson=27.6mOHM



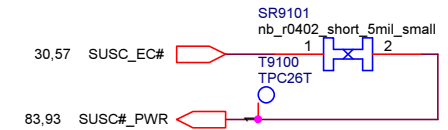
VGS=10V, RDson=27.6mOHM



## SUSB#\_PWR POWER Control



## SUSC#\_PWR POWER Control



<Variant Name>

<b>PEGATRON</b>		Title : <b>SWITCH</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
Engineer:		<b>Neil Lin</b>	
Size <i>Custom</i>	Project Name <b>AS3EA</b>	Rev <b>2.0</b>	
Date: <b>Monday, March 27, 2017</b>	Sheet	<b>91</b>	of <b>100</b>





**Engineer:** **Neil Lin**

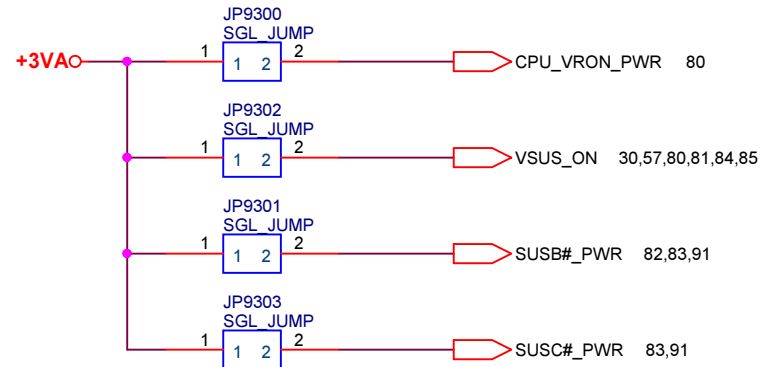
Date:	Monday, March 27, 2017	Sheet	92	of	100
-------	------------------------	-------	----	----	-----

+A/D\_DOCK\_IN ➡ +A/D\_DOCK\_IN 60,88  
+AC\_BAT\_SYS ➡ +AC\_BAT\_SYS 45,80,81,83,88  
+BAT\_CON ➡ +BAT\_CON 60,88  
  
+5VA ➡ +5VA 57,66,81  
+3VA ➡ +3VA 9,30,31,36,53,60,65,81,88

+5VO ➡ +5VO 80,81,83,84,88,91  
+3VO ➡ +3VO 81,82,85,91  
+1.8VO ➡ +1.8VO 84,91  
+1.24VO ➡ +1.24VO 85  
+VDDQVO ➡ +VDDQVO 83  
+1.05VO ➡ +1.05VO 82  
+0.675VO ➡ +0.675VO 83  
  
+12VSUS ➡ +12VSUS 6,81,91  
+3VSUS ➡ +3VSUS 4,6,7,9,12,15,30,31,45,53,57,62,80,81,84,85,92  
+5VSUS ➡ +5VSUS 41,52,66,81  
+1.8VSUS ➡ +1.8VSUS 4,5,6,7,8,9,12,13,15,44,57,84  
+1.24VSUS ➡ +1.24VSUS 9,57,85

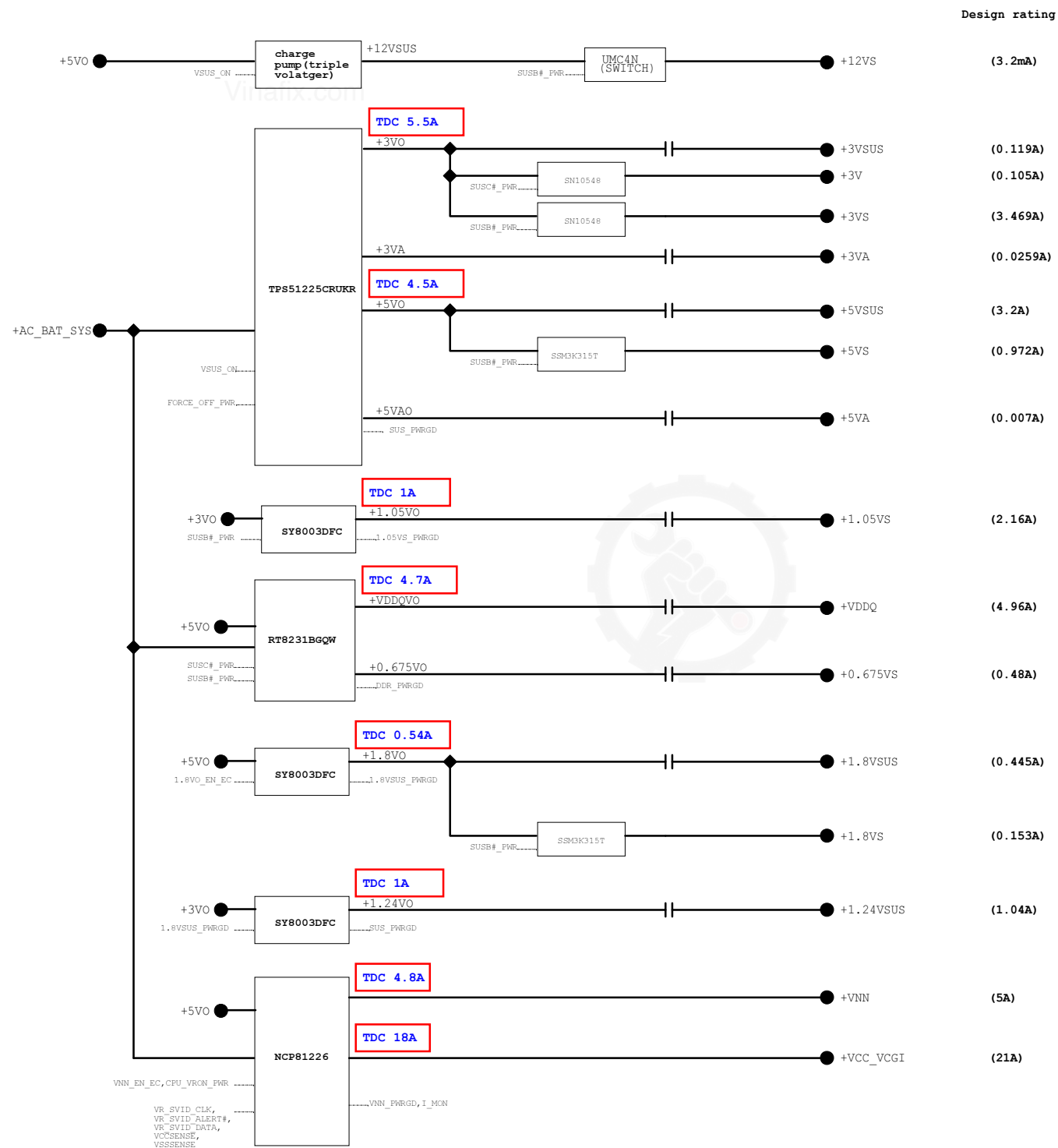
+VDDQ ➡ +VDDQ 9,16,17,18,57,83  
+12VS ➡ +12VS 31,49,57,91  
+5VS ➡ +5VS 31,36,48,57,69,91  
+3VS ➡ +3VS 6,12,30,31,32,36,37,41,45,48,49,50,51,53,57,62,66,91,92  
+1.8VS ➡ +1.8VS 4,5,6,12,31,32,36,48,49,91  
+1.05VS ➡ +1.05VS 4,9,57,82  
+0.675VS ➡ +0.675VS 16,17,57,83  
  
+VNN ➡ +VNN 9,57,80  
+VCORE ➡ +VCORE 9,57,80  
+3VA\_EC ➡ +3VA\_EC 15,30,32,80

## FOR POWER TEST



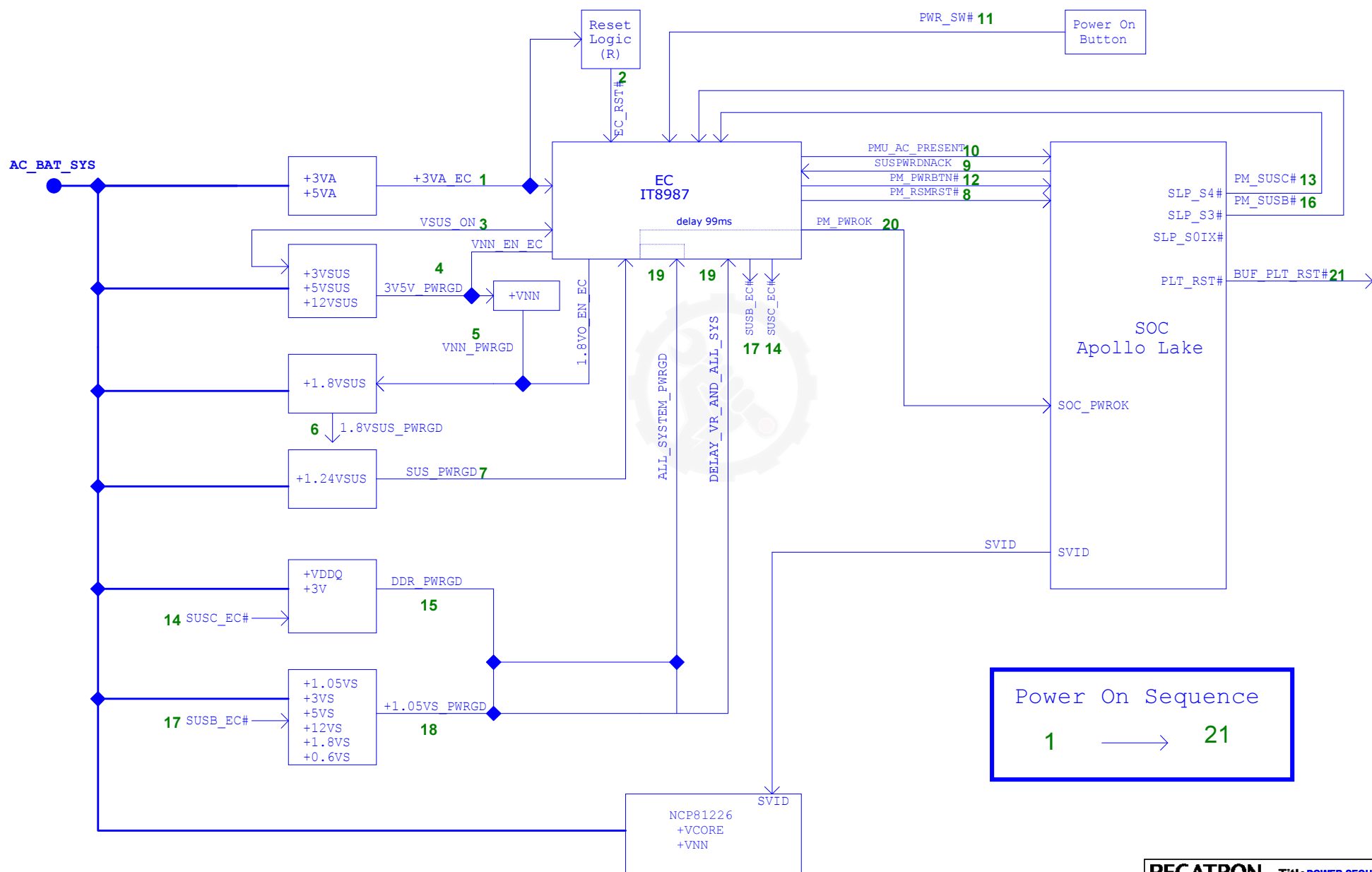
<Variant Name>

<b>PEGATRON</b>		Title : <b>SIGNAL</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
Engineer: <b>Neil Lin</b>			
Size <b>A4</b>	Project Name <b>AS3EA</b>		Rev <b>2.0</b>
Date: <b>Monday, March 27, 2017</b>	Sheet <b>93</b> of <b>100</b>		



# Power On Sequence Diagram G3-S0 R0.1

Vinafix.com



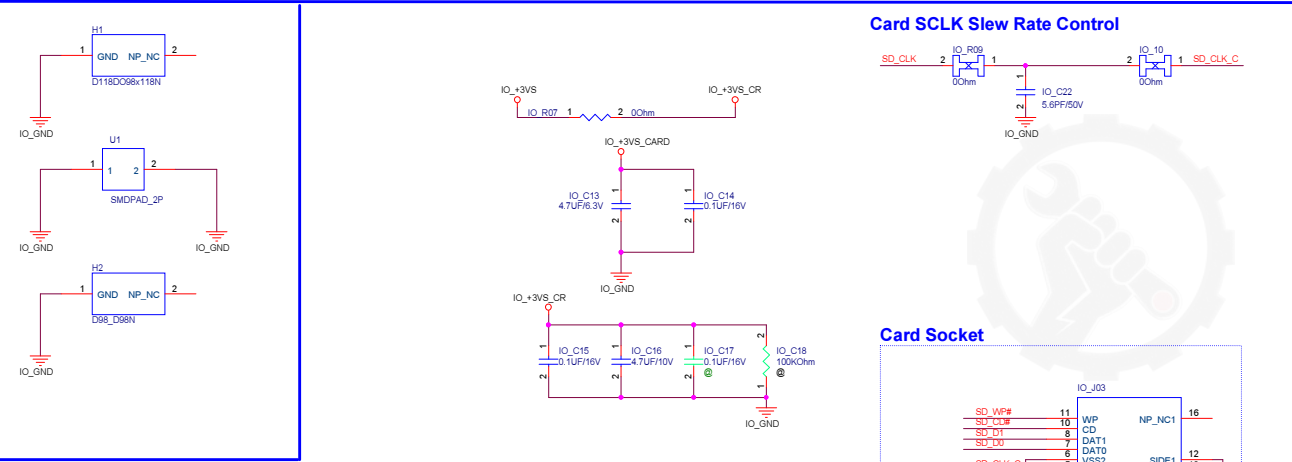
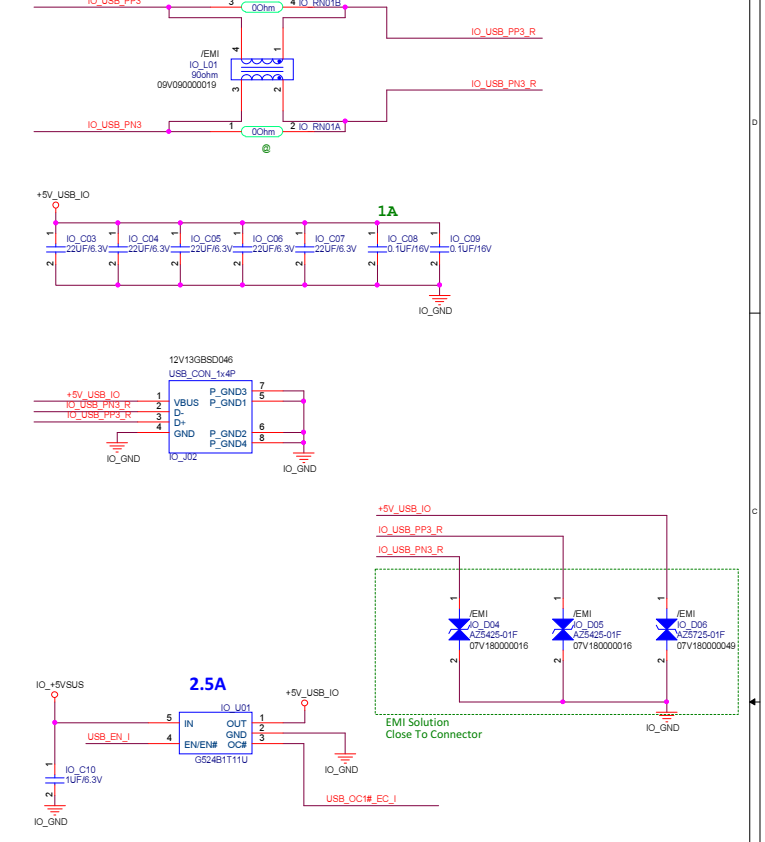
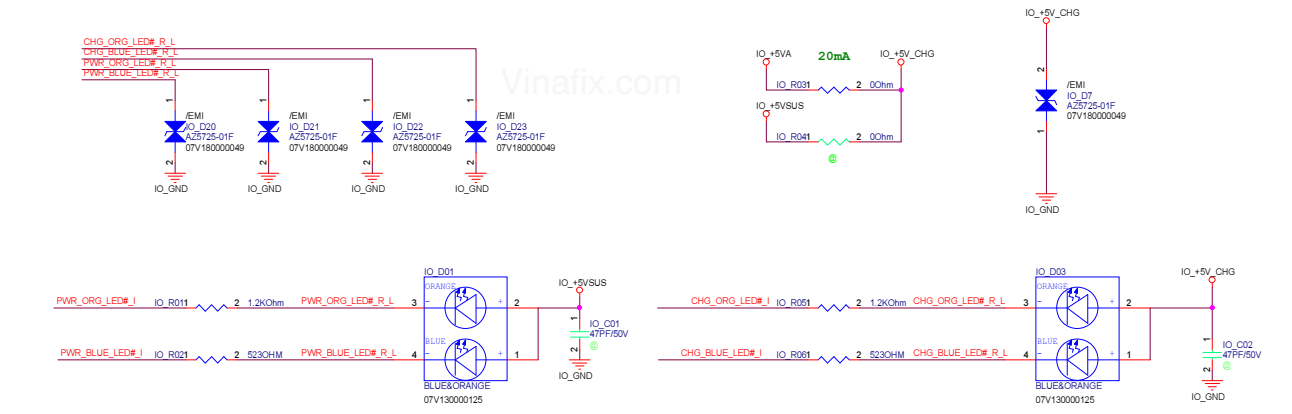
Power On Sequence

1 → 21

LED POWER LED

Charger LED

USB 2.0



Connector

